PIC16C5X

EPROM/ROM-Based 8-Bit CMOS Microcontroller Series

Devices Included in this Data Sheet:

- PIC16C52
- PIC16C54s
- PIC16CR54s
- PIC16C55s
- PIC16C56s
- PIC16CR56s
- PIC16C57s
- PIC16CR57s
- PIC16C58s
- PIC16CR58s

Note:	The letter "s" used following the part numbers throughout this document indicate plural, meaning there is more than one part variety for the indicated device.

High-Performance RISC CPU:

- Only 33 single word instructions to learn
- All instructions are single cycle (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle

Device	Pins	I/O	EPROM/ ROM	RAM
PIC16C52	18	12	384	25
PIC16C54	18	12	512	25
PIC16C54A	18	12	512	25
PIC16C54B	18	12	512	25
PIC16C54C	18	12	512	25
PIC16CR54A	18	12	512	25
PIC16CR54B	18	12	512	25
PIC16CR54C	18	12	512	25
PIC16C55	28	20	512	24
PIC16C55A	28	20	512	24
PIC16C56	18	12	1K	25
PIC16C56A	18	12	1K	25
PIC16CR56A	18	12	1K	25
PIC16C57	28	20	2K	72
PIC16C57C	28	20	2K	72
PIC16CR57B	28	20	2K	72
PIC16CR57C	28	20	2K	72
PIC16C58A	18	12	2K	73
PIC16C58B	18	12	2K	73
PIC16CR58A	18	12	2K	73
PIC16CR58B	18	12	2K	73

- 12-bit wide instructions
- 8-bit wide data path
- Seven or eight special function hardware registers
- Two-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features:

- 8-bit real time clock/counter (TMR0) with 8-bit programmable prescaler
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options:
  - RC: Low-cost RC oscillator
  - XT: Standard crystal/resonator
  - HS: High-speed crystal/resonator
  - LP: Power saving, low-frequency crystal

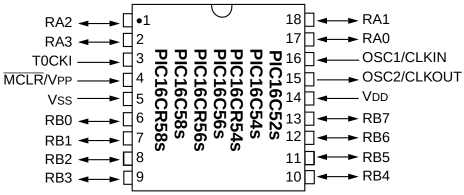
CMOS Technology:

- Low-power, high-speed CMOS EPROM/ROM technology
- Fully static design
- Wide-operating voltage and temperature range:
  - EPROM Commercial/Industrial 2.0V to 6.25V
  - ROM Commercial/Industrial 2.0V to 6.25V
  - EPROM Extended 2.5V to 6.0V
  - ROM Extended 2.5V to 6.0V
- Low-power consumption
  - < 2 mA typical @ 5V, 4 MHz
  - 15 μA typical @ 3V, 32 kHz
  - < 0.6 μA typical standby current (with WDT disabled) @ 3V, 0°C to 70°C

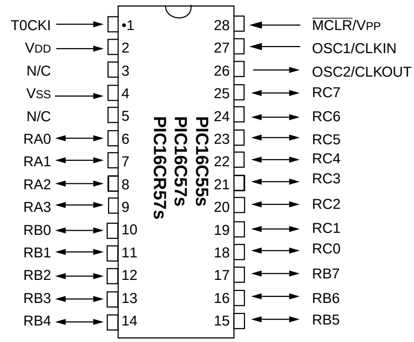
Note:	In this document, figure and table titles refer to all varieties of the part number indicated, (i.e., The title "Figure 14-1: Load Conditions - PIC16C54A", also refers to PIC16LC54A and PIC16LV54A parts).

Pin Diagrams

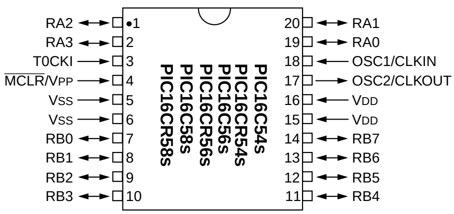
PDIP, SOIC, Windowed CERDIP



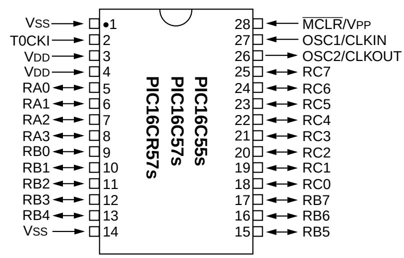
PDIP, SOIC, Windowed CERDIP



SSOP



SSOP



Device Differences

Device	Voltage Range	Oscillator Selection (Program)	Oscillator	Process Technology (Microns)	ROM Equivalent	$\overline{MCLR}$ Filter
PIC16C52	3.0-6.25	User	See Note 1	0.9	—	No
PIC16C54	2.5-6.25	Factory	See Note 1	1.2	PIC16CR54A	No
PIC16C54A	2.0-6.25	User	See Note 1	0.9	—	No
PIC16C54B	2.5-5.5	User	See Note 1	0.7	PIC16CR54B	Yes
PIC16C54C	2.5-5.5	User	See Note 1	0.7	PIC16CR54C	Yes
PIC16C55	2.5-6.25	Factory	See Note 1	1.7	—	No
PIC16C55A	2.5-5.5	User	See Note 1	0.7	—	Yes
PIC16C56	2.5-6.25	Factory	See Note 1	1.7	—	No
PIC16C56A	2.5-5.5	User	See Note 1	0.7	PIC16CR56A	Yes
PIC16C57	2.5-6.25	Factory	See Note 1	1.2	—	No
PIC16C57C	2.5-5.5	User	See Note 1	0.7	PIC16CR57C	Yes
PIC16C58A	2.0-6.25	User	See Note 1	0.9	PIC16CR58A	No(2)
PIC16C58B	2.5-5.5	User	See Note 1	0.7	PIC16CR58B	Yes
PIC16CR54A	2.5-6.25	Factory	See Note 1	1.2	N/A	Yes
PIC16CR54B	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR54C	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR56A	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR57B	2.5-6.25	Factory	See Note 1	0.9	N/A	Yes
PIC16CR57C	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR58A	2.5-6.25	Factory	See Note 1	0.9	N/A	Yes
PIC16CR58B	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

Note 2: In PIC16LV58A, $\overline{MCLR}$ Filter = Yes

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Errata

An errata sheet may exist for current devices, describing minor operational differences (from the data sheet) and recommended workarounds. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)
- The Microchip Corporate Literature Center; U.S. FAX: (602) 786-7277

When contacting a sales office or the literature center, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Corrections to this Data Sheet

We constantly strive to improve the quality of all our products and documentation. We have spent a great deal of time to ensure that this document is correct. However, we realize that we may have missed a few things. If you find any information that is missing or appears in error, please:

- Fill out and mail in the reader response form in the back of this data sheet.
- E-mail us at webmaster@microchip.com.

We appreciate your assistance in making this a better document.

 Preliminary

1.0 GENERAL DESCRIPTION

The PIC16C5X from Microchip Technology is a family of low-cost, high performance, 8-bit, fully static, EPROM/ ROM-based CMOS microcontrollers. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle (200 ns) except for program branches which take two cycles. The PIC16C5X delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C5X products are equipped with special features that reduce system cost and power requirements. The Power-On Reset (POR) and Device Reset Timer (DRT) eliminate the need for external reset circuitry. There are four oscillator configurations to choose from, including the power-saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The UV erasable CERDIP packaged versions are ideal for code development, while the cost-effective One Time Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers while benefiting from the OTP's flexibility.

The PIC16C5X products are supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, fuzzy logic support tools, a low-cost development programmer, and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The PIC16C5X series fits perfectly in applications ranging from high-speed automotive and appliance motor control to low-power remote transmitters/receivers, pointing devices and telecom processors. The EPROM technology makes customizing application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC16C5X series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, coprocessor applications).

TABLE 1-1: PIC16C5X FAMILY OF DEVICES

		PIC16C52	PIC16C54s	PIC16CR54s	PIC16C55s	PIC16C56s
Clock	Maximum Frequency of Operation (MHz)	4	20	20	20	20
Memory	EPROM Program Memory (x12 words)	384	512	—	512	1K
	ROM Program Memory (x12 words)	—	—	512	—	—
	RAM Data Memory (bytes)	25	25	25	24	25
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0
Features	I/O Pins	12	12	12	20	12
	Number of Instructions	33	33	33	33	33
	Packages	18-pin DIP, SOIC	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP

All PICmicro™ Family devices have Power-on Reset, selectable Watchdog Timer (except PIC16C52), selectable code protect and high I/O current capability.

		PIC16CR56s	PIC16C57s	PIC16CR57s	PIC16C58s	PIC16CR58s
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	20
Memory	EPROM Program Memory (x12 words)	—	2K	—	2K	—
	ROM Program Memory (x12 words)	1K	—	2K	—	2K
	RAM Data Memory (bytes)	25	72	72	73	73
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0
Features	I/O Pins	12	20	20	12	12
	Number of Instructions	33	33	33	33	33
	Packages	18-pin DIP, SOIC; 20-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP

All PICmicro™ Family devices have Power-on Reset, selectable Watchdog Timer (except PIC16C52), selectable code protect and high I/O current capability.

2.0 PIC16C5X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC16C5X Product Identification System at the back of this data sheet to specify the correct part number.

For the PIC16C5X family of devices, there are four device types, as indicated in the device number:

1. **C**, as in PIC16C54. These devices have EPROM program memory and operate over the standard voltage range.
2. **LC**, as in PIC16LC54A. These devices have EPROM program memory and operate over an extended voltage range.
3. **LV**, as in PIC16LV54A. These devices have EPROM program memory and operate over a 2.0V to 3.8V range.
4. **CR**, as in PIC16CR54A. These devices have ROM program memory and operate over the standard voltage range.
5. **LCR**, as in PIC16LCR54B. These devices have ROM program memory and operate over an extended voltage range.

2.1 UV Erasable Devices (EPROM)

The UV erasable versions, offered in CERDIP packages, are optimal for prototype development and pilot programs

UV erasable devices can be programmed for any of the four oscillator configurations. Microchip's PICSTART® and PRO MATE® programmers both support programming of the PIC16C5X. Third party programmers also are available; refer to the Third Party Guide for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production (SQTP SM) Devices

Microchip offers the unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number.

2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, giving the customer a low cost option for high volume, mature products.

NOTES:

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12-bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (200ns @ 20MHz) except for program branches.

The PIC16C52 addresses 384 x 12 of program memory, the PIC16C54s/CR54s and PIC16C55s address 512 x 12 of program memory, the PIC16C56s/CR56s address 1K X 12 of program memory, and the PIC16C57s/CR57s and PIC16C58s/CR58s address 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of ‘special optimal situations’ make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C5X device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

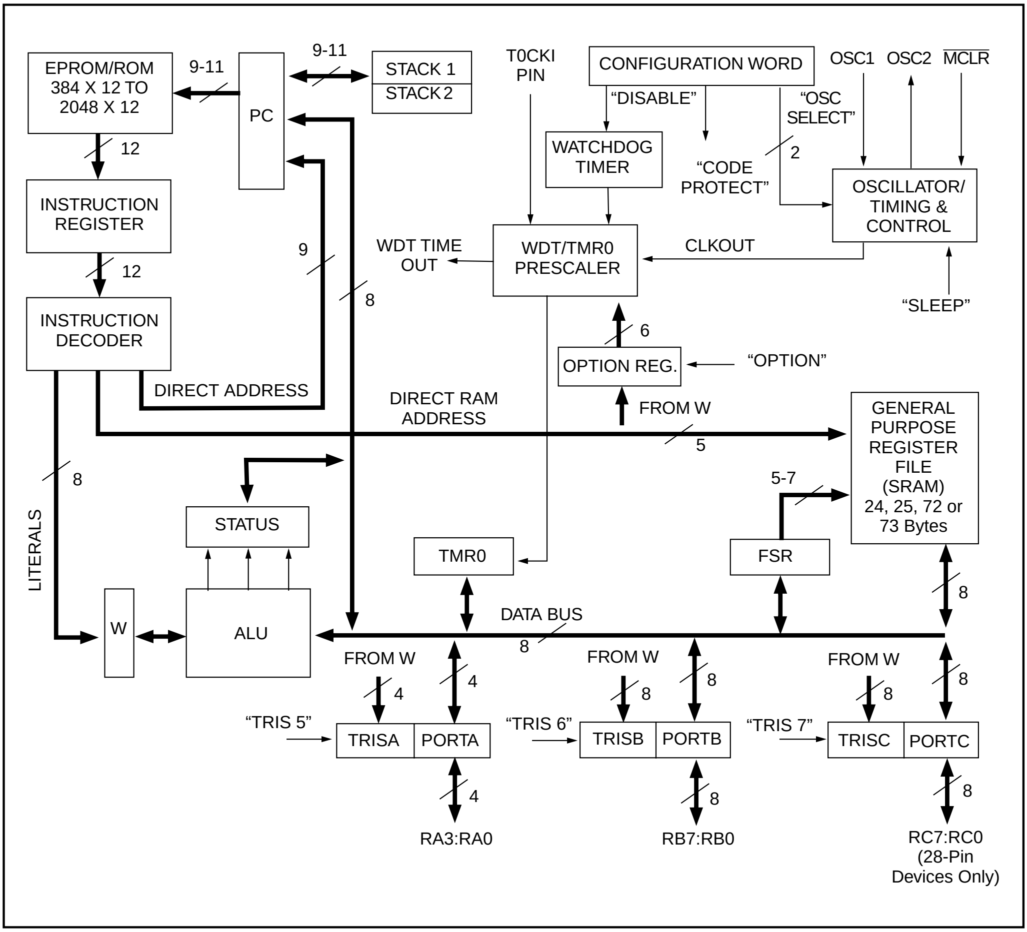
The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the `SUBWF` and `ADDWF` instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1.

FIGURE 3-1: PIC16C5X SERIES BLOCK DIAGRAM



 Preliminary

TABLE 3-1: PINOUT DESCRIPTION - PIC16C52, PIC16C54s, PIC16CR54s, PIC16C56s, PIC16CR56s, PIC16C58s, PIC16CR58s

Name	DIP, SOIC No.	SSOP No.	I/O/P Type	Input Levels	Description
RA0 RA1 RA2 RA3	17 18 1 2	19 20 1 2	I/O I/O I/O I/O	TTL TTL TTL TTL	Bi-directional I/O port
RB0 RB1 RB2 RB3 RB4 RB5 RB6 RB7	6 7 8 9 10 11 12 13	7 8 9 10 11 12 13 14	I/O I/O I/O I/O I/O I/O I/O I/O	TTL TTL TTL TTL TTL TTL TTL TTL	Bi-directional I/O port
T0CKI	3	3	I	ST	Clock input to Timer0. Must be tied to V_{SS} or V_{DD}, if not in use, to reduce current consumption.
$\overline{MCLR}/V_{PP}$	4	4	I	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device. Voltage on the $\overline{MCLR}/V_{PP}$ pin must not exceed V_{DD} to avoid unintended entering of programming mode.
OSC1/CLKIN	16	18	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	17	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
V_{DD}	14	15,16	P	—	Positive supply for logic and I/O pins.
V_{SS}	5	5,6	P	—	Ground reference for logic and I/O pins.

Legend: I = input, O = output, I/O = input/output,
P = power, — = Not Used, TTL = TTL input,
ST = Schmitt Trigger input

TABLE 3-2: PINOUT DESCRIPTION - PIC16C55s, PIC16C57s, PIC16CR57s

Name	DIP, SOIC No.	SSOP No.	I/O/P Type	Input Levels	Description
RA0 RA1 RA2 RA3	6 7 8 9	5 6 7 8	I/O I/O I/O I/O	TTL TTL TTL TTL	Bi-directional I/O port
RB0 RB1 RB2 RB3 RB4 RB5 RB6 RB7	10 11 12 13 14 15 16 17	9 10 11 12 13 15 16 17	I/O I/O I/O I/O I/O I/O I/O I/O	TTL TTL TTL TTL TTL TTL TTL TTL	Bi-directional I/O port
RC0 RC1 RC2 RC3 RC4 RC5 RC6 RC7	18 19 20 21 22 23 24 25	18 19 20 21 22 23 24 25	I/O I/O I/O I/O I/O I/O I/O I/O	TTL TTL TTL TTL TTL TTL TTL TTL	Bi-directional I/O port
T0CKI	1	2	I	ST	Clock input to Timer0. Must be tied to V_{SS} or V_{DD} if not in use to reduce current consumption.
$\overline{MCLR}$	28	28	I	ST	Master clear (reset) input. This pin is an active low reset to the device.
OSC1/CLKIN	27	27	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	26	26	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
V_{DD}	2	3,4	P	—	Positive supply for logic and I/O pins.
V_{SS}	4	1,14	P	—	Ground reference for logic and I/O pins.
N/C	3,5	—	—	—	Unused, do not connect

Legend: I = input, O = output, I/O = input/output,
P = power, — = Not Used,
TTL = TTL input, ST = Schmitt Trigger input

 Preliminary

3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1, and the instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2 and Example 3-1.

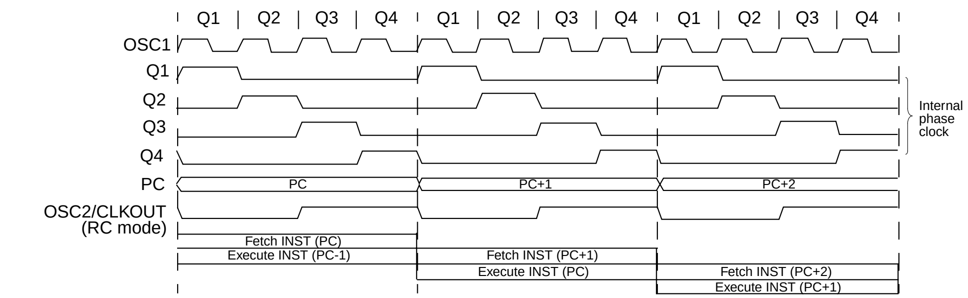
3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., `GOTO`) then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW

`1. MOVLW 55H`	Fetch 1	Execute 1				
`2. MOVWF PORTB`		Fetch 2	Execute 2			
`3. CALL  SUB_1`			Fetch 3	Execute 3		
`4. BSF   PORTA, BIT3`				Fetch 4	Flush	
					Fetch SUB_1	Execute SUB_1

All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is “flushed” from the pipeline while the new instruction is being fetched and then executed.

NOTES:

4.0 MEMORY ORGANIZATION

PIC16C5X memory is organized into program memory and data memory. For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using one or two STATUS register bits. For devices with a data memory register file of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Selection Register (FSR).

4.1 Program Memory Organization

The PIC16C52 has a 9-bit Program Counter (PC) capable of addressing a 384 x 12 program memory space (Figure 4-1). The PIC16C54s, PIC16CR54s and PIC16C55s have a 9-bit Program Counter (PC) capable of addressing a 512 x 12 program memory space (Figure 4-2). The PIC16C56s and PIC16CR56s have a 10-bit Program Counter (PC) capable of addressing a 1K x 12 program memory space (Figure 4-3). The PIC16CR57s, PIC16C58s and PIC16CR58s have an 11-bit Program Counter capable of addressing a 2K x 12 program memory space (Figure 4-4). Accessing a location above the physically implemented address will cause a wraparound.

The reset vector for the PIC16C52 is at 17Fh. A NOP at the reset vector location will cause a restart at location 000h. The reset vector for the PIC16C54s, PIC16CR54s and PIC16C55s is at 1FFh. The reset vector for the PIC16C56s and PIC16CR56s is at 3FFh. The reset vector for the PIC16C57s, PIC16CR57s, PIC16C58s, and PIC16CR58s is at 7FFh.

FIGURE 4-1: PIC16C52 PROGRAM MEMORY MAP AND STACK

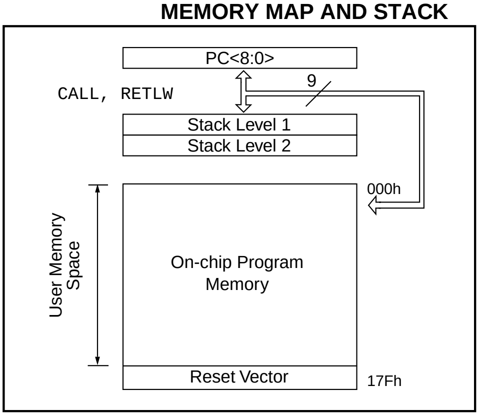


FIGURE 4-2: PIC16C54s/CR54s/C55s PROGRAM MEMORY MAP AND STACK

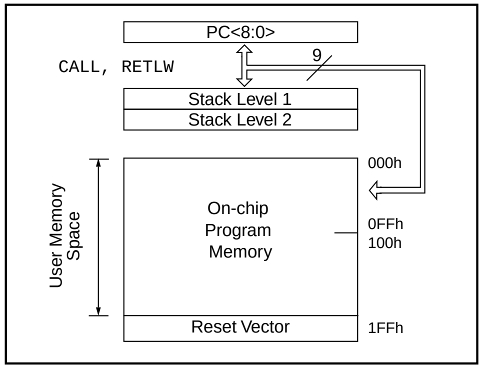


FIGURE 4-3: PIC16C56s/CR56s PROGRAM MEMORY MAP AND STACK

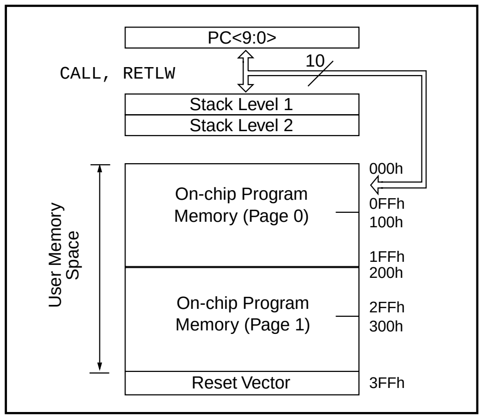
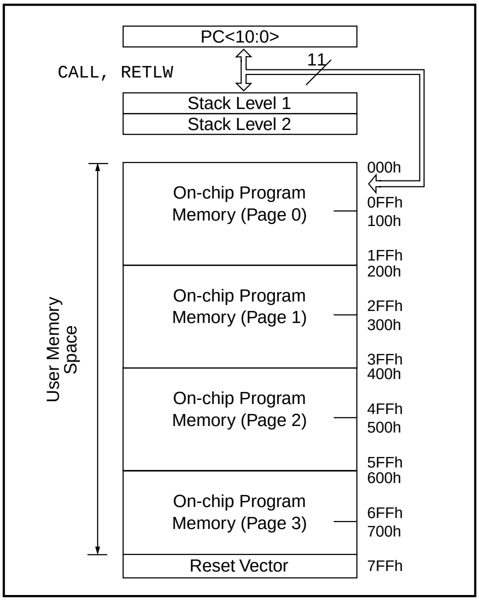


FIGURE 4-4: PIC16C57s/CR57s/C58s/CR58s PROGRAM MEMORY MAP AND STACK



4.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: special function registers and general purpose registers.

The special function registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports), and the File Select Register (FSR). In addition, special purpose registers are used to control the I/O port configuration and prescaler options.

The general purpose registers are used for data and control information under command of the instructions.

For the PIC16C52, PIC16C54s, PIC16CR54s, PIC16C56s and PIC16CR56s, the register file is composed of 7 special function registers and 25 general purpose registers (Figure 4-5).

For the PIC16C55s, the register file is composed of 8 special function registers and 24 general purpose registers.

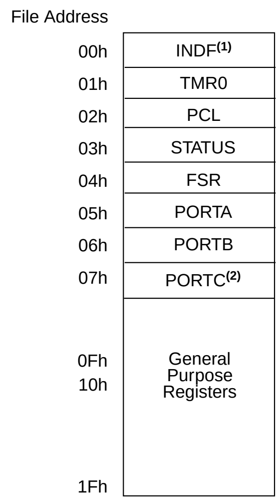
For the PIC16C57s and PIC16CR57s, the register file is composed of 8 special function registers, 24 general purpose registers and up to 48 additional general purpose registers that may be addressed using a banking scheme (Figure 4-6).

For the PIC16C58s and PIC16CR58s, the register file is composed of 7 special function registers, 25 general purpose registers and up to 48 additional general purpose registers that may be addressed using a banking scheme (Figure 4-7).

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is accessed either directly or indirectly through the file select register FSR (Section 4.7).

FIGURE 4-5: PIC16C52, PIC16C54s, PIC16CR54s, PIC16C55s, PIC16C56s, PIC16CR56s REGISTER FILE MAP



Note 1: Not a physical register. See Section 4.7
2: PIC16C55s only, others are a general purpose register.

FIGURE 4-6: PIC16C57s/CR57s REGISTER FILE MAP

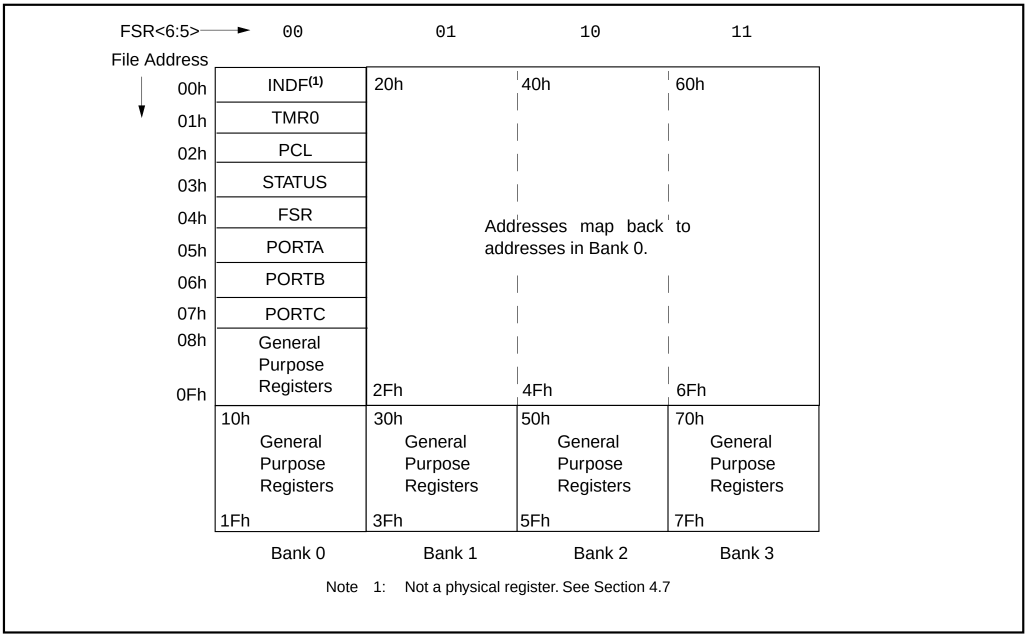
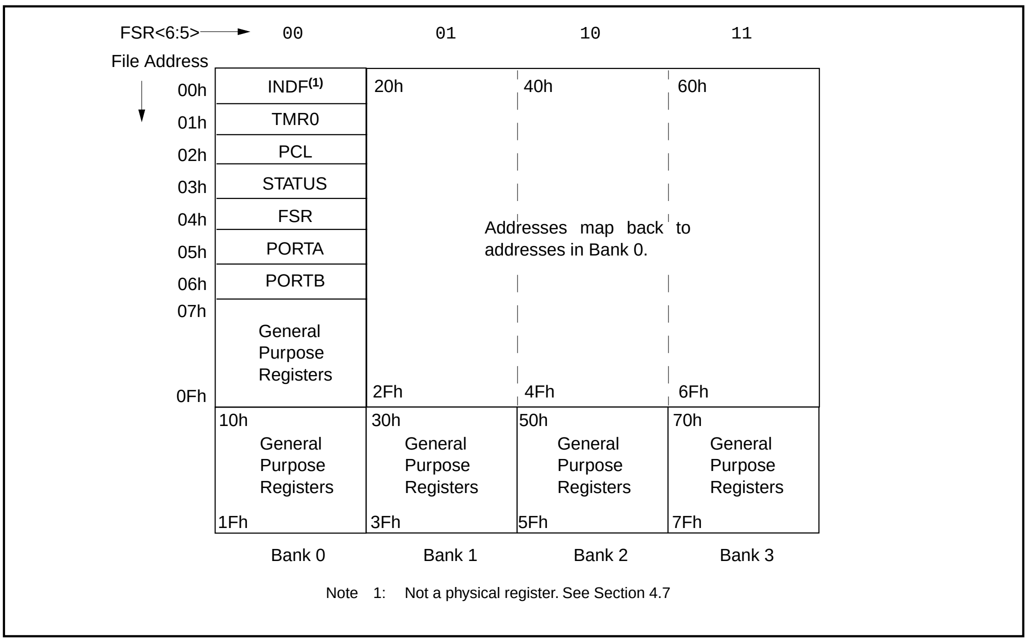


FIGURE 4-7: PIC16C58s/CR58s REGISTER FILE MAP



4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The special registers can be classified into two sets. The special function registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{\text{MCLR}}$ and WDT Reset
N/A	TRIS	I/O control registers (TRISA, TRISB, TRISC)								1111 1111	1111 1111
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT prescaler								--11 1111	--11 1111
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
02h(1)	PCL	Low order 8 bits of PC								1111 1111	1111 1111
03h	STATUS	PA2	PA1	PA0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect data memory address pointer								1xxx xxxx	1uuu uuuu
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h(2)	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu

Legend: Shaded boxes = unimplemented or unused, – = unimplemented, read as '0' (if applicable)
x = unknown, u = unchanged, q = see the tables in Section 7.7 for possible values.

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 4.5 for an explanation of how to access these bits.

2: File address 07h is a general purpose register on the PIC16C52, PIC16C54s, PIC16CR54s, PIC16C56s, PIC16CR56s, PIC16C58s and PIC16CR58s.

4.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bits for program memories larger than 512 words.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS register because these instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions, which do affect STATUS bits, see Section 8.0, Instruction Set Summary.

FIGURE 4-8: STATUS REGISTER (ADDRESS:03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7	6	5	4	3	2	1	bit0

R = Readable bit
W = Writable bit
- n = Value at POR reset

bit 7: **PA2**: This bit unused at this time.
Use of the PA2 bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

bit 6-5: **PA1:PA0**: Program page preselect bits (PIC16C56s/CR56s)(PIC16C57s/CR57s)(PIC16C58s/CR58s)
00 = Page 0 (000h - 1FFh) - PIC16C56s/CR56s, PIC16C57s/CR57s, PIC16C58s/CR58s
01 = Page 1 (200h - 3FFh) - PIC16C56s/CR56s, PIC16C57s/CR57s, PIC16C58s/CR58s
10 = Page 2 (400h - 5FFh) - PIC16C57s/CR57s, PIC16C58s/CR58s
11 = Page 3 (600h - 7FFh) - PIC16C57s/CR57s, PIC16C58s/CR58s
Each page is 512 words.
Using the PA1:PA0 bits as general purpose read/write bits in devices which do not use them for program page preselect is not recommended since this may affect upward compatibility with future products.

bit 4: **$\overline{TO}$**: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3: **$\overline{PD}$**: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (for `ADDWF` and `SUBWF` instructions)
ADDWF
1 = A carry from the 4th low order bit of the result occurred
0 = A carry from the 4th low order bit of the result did not occur
SUBWF
1 = A borrow from the 4th low order bit of the result did not occur
0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C**: Carry/$\overline{borrow}$ bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)

ADDWF	**SUBWF**	**RRF or RLF**
1 = A carry occurred	1 = A borrow did not occur	Load bit with LSb or MSb, respectively
0 = A carry did not occur	0 = A borrow occurred	

4.4 OPTION Register

The OPTION register is a 6-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W register will be transferred to the OPTION register. A RESET sets the OPTION<5:0> bits.

FIGURE 4-9: OPTION REGISTER

U-0	U-0	W-1	W-1	W-1	W-1	W-1	W-1
—	—	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7	6	5	4	3	2	1	bit0

W = Writable bit
U = Unimplemented bit
- n = Value at POR reset

bit 7-6: **Unimplemented**.

bit 5: **T0CS**: Timer0 clock source select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: Timer0 source edge select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3: **PSA**: Prescaler assignment bit
1 = Prescaler assigned to the WDT (not implemented on PIC16C52)
0 = Prescaler assigned to Timer0

bit 2-0: **PS2:PS0**: Prescaler rate select bits

Bit Value	Timer0 Rate	WDT Rate (not implemented on PIC16C52)
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

4.5 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

For a `GOTO` instruction, bits 8:0 of the PC are provided by the `GOTO` instruction word. The PC Latch (PCL) is mapped to PC<7:0> (Figure 4-10 and Figure 4-11).

For the PIC16C56s, PIC16CR56s, PIC16C57s, PIC16CR57s, PIC16C58s and PIC16CR58s, a page number must be supplied as well. Bit5 and bit6 of the STATUS register provide page information to bit9 and bit10 of the PC (Figure 4-11 and Figure 4-12).

For a `CALL` instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-10 and Figure 4-11).

Instructions where the PCL is the destination, or Modify PCL instructions, include `MOVWF PC, ADDWF PC,` and `BSF PC,5.`

For the PIC16C56s, PIC16CR56s, PIC16C57s, PIC16CR57s, PIC16C58s and PIC16CR58s, a page number again must be supplied. Bit5 and bit6 of the STATUS register provide page information to bit9 and bit10 of the PC (Figure 4-11 and Figure 4-12).

Note:	Because PC<8> is cleared in the `CALL` instruction, or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-10: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C52, PIC16C54s, PIC16CR54s, PIC16C55s

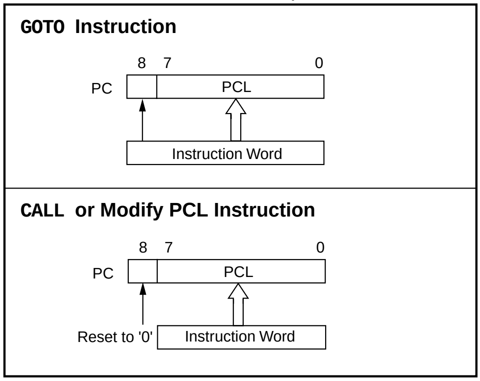


FIGURE 4-11: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C56s/PIC16CR56s

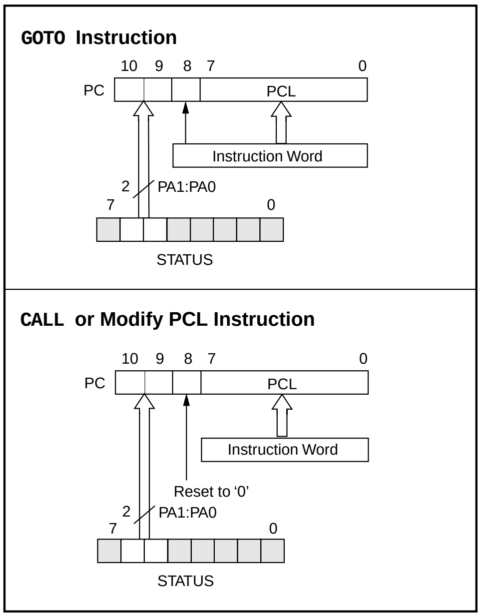
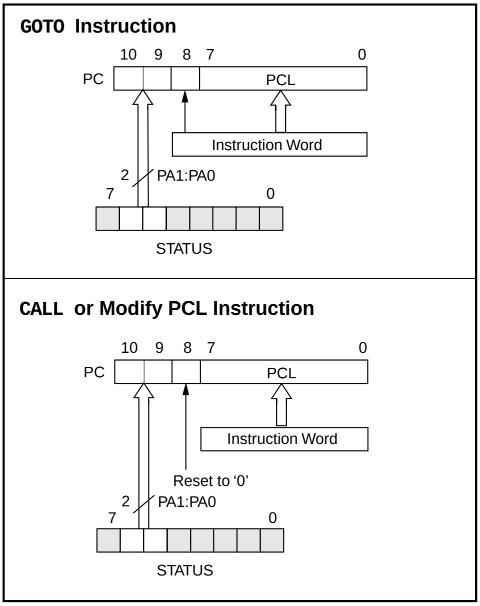


FIGURE 4-12: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C57s/PIC16CR57s, AND PIC16C58s/PIC16CR58s



4.5.1 PAGING CONSIDERATIONS – PIC16C56s/CR56s, PIC16C57s/CR57s AND PIC16C58s/CR58s

If the Program Counter is pointing to the last address of a selected memory page, when it increments it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS register will not be updated. Therefore, the next `GOTO`, `CALL`, or Modify PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA1:PA0).

For example, a `NOP` at location 1FFh (page 0) increments the PC to 200h (page 1). A `GOTO xxx` at 200h will return the program to address 0xxh on page 0 (assuming that PA1:PA0 are clear).

To prevent this, the page preselect bits must be updated under program control.

4.5.2 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page i.e., the reset vector.

The STATUS register page preselect bits are cleared upon a RESET, which means that page 0 is pre-selected.

Therefore, upon a RESET, a `GOTO` instruction at the reset vector location will automatically cause the program to jump to page 0.

4.6 Stack

PIC16C5X devices have a 9-bit, 10-bit or 11-bit wide, two-level hardware push/pop stack (Figure 4-2, Figure 4-1, and Figure 4-3 respectively).

A `CALL` instruction will *push* the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential `CALL`'s are executed, only the most recent two return addresses are stored.

A `RETLW` instruction will *pop* the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential `RETLW`'s are executed, the stack will be filled with the address previously stored in level 2. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

For the `RETLW` instruction, the PC is loaded with the Top Of Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC.

4.7 Indirect Data Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 4-1: INDIRECT ADDRESSING

- Register file 05 contains the value 10h
- Register file 06 contains the value 0Ah
- Load the value 05 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 06h)
- A read of the INDR register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
          movlw   0x10    ;initialize pointer
          movwf   FSR     ; to RAM
NEXT      clrf    INDF    ;clear INDF register
          incf    FSR,F   ;inc pointer
          btfsc   FSR,4   ;all done?
          goto    NEXT    ;NO, clear next
CONTINUE
          :               ;YES, continue
```

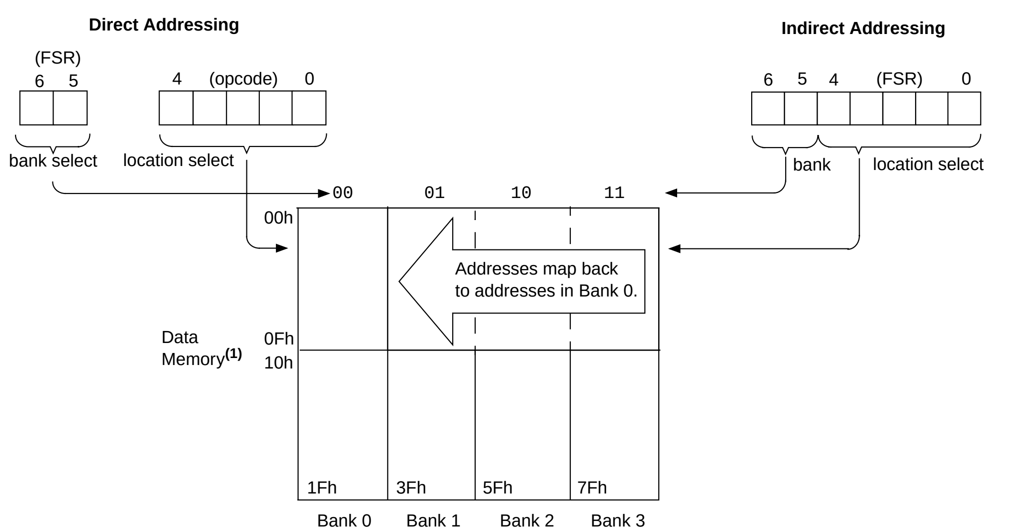
The FSR is either a 5-bit (PIC16C52, PIC16C54s, PIC16CR54s, PIC16C55s), 6-bit (PIC16C56s, PIC16CR56s), or 7-bit (PIC16C57s, PIC16CR57s, PIC16C58s, PIC16CR58s) wide register. It is used in conjunction with the INDF register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC16C52, PIC16C54s, PIC16CR54s, PIC16C55s: These do not use banking. FSR<6:5> are unimplemented and read as '1's.

PIC16C57s, PIC16CR57s, PIC16C58s, PIC16CR58s: FSR<6:5> are the bank select bits and are used to select the bank to be addressed (`00` = bank 0, `01` = bank 1, `10` = bank 2, `11` = bank 3).

FIGURE 4-13: DIRECT/INDIRECT ADDRESSING



Note 1: For register map detail see Section 4.2.

5.0 I/O PORTS

As with any other register, the I/O registers can be written and read under program control. However, read instructions (e.g., `MOVF PORTB,W`) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

5.1 PORTA

PORTA is a 4-bit I/O register. Only the low order 4 bits are used (RA3:RA0). Bits 7-4 are unimplemented and read as '0's.

5.2 PORTB

PORTB is an 8-bit I/O register (PORTB<7:0>).

5.3 PORTC

PORTC is an 8-bit I/O register for PIC16C55s, PIC16C57s and PIC16CR57s.

PORTC is a general purpose register for PIC16C52, PIC16C54s, PIC16CR54s, PIC16C56s, PIC16C58s and PIC16CR58s.

5.4 TRIS Registers

The output driver control registers are loaded with the contents of the W register by executing the `TRIS f` instruction. A '1' from a TRIS register bit puts the corresponding output driver in a hi-impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

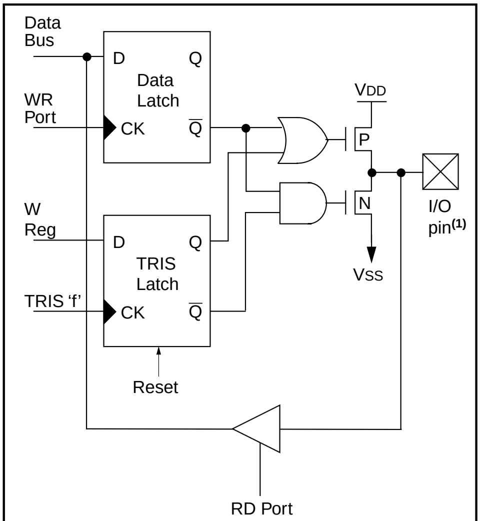
> **Note:** A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.

The TRIS registers are "write-only" and are set (output drivers disabled) upon RESET.

5.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 5-1. All ports may be used for both input and output operation. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., `MOVF PORTB, W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

FIGURE 5-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



Note 1: I/O pins have protection diodes to VDD and VSS.

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
N/A	TRIS	I/O control registers (TRISA, TRISB, TRISC)								1111 1111	1111 1111
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu

Legend: Shaded boxes = unimplemented, read as '0',
– = unimplemented, read as '0', x = unknown, u = unchanged

5.6 I/O Programming Considerations

5.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin (“wired-or”, “wired-and”). The resulting high output currents may damage the chip.

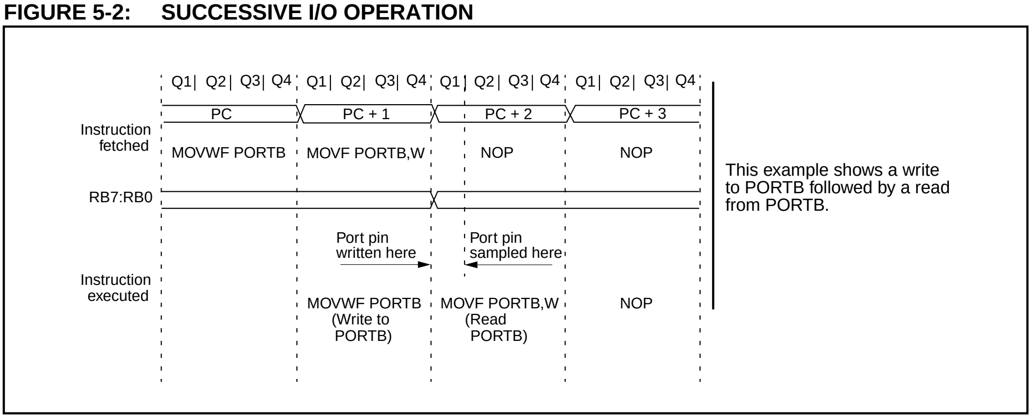
EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                   PORT latch  PORT pins
;                   ----------  ----------
  BCF   PORTB, 7   ;01pp pppp   11pp pppp
  BCF   PORTB, 6   ;10pp pppp   11pp pppp
  MOVLW 03Fh       ;
  TRIS  PORTB      ;10pp pppp   10pp pppp
;
;Note that the user may have expected the pin
;values to be 00pp pppp. The 2nd BCF caused
;RB7 to be latched as the pin value (High).
```

5.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 5-2: SUCCESSIVE I/O OPERATION



 Preliminary

6.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
  - Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
  - Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module, while Figure 6-2 shows the electrical structure of the Timer0 input.

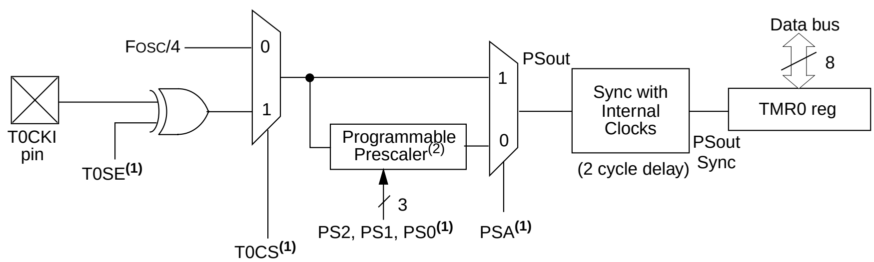
Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-3 and Figure 6-4). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.1.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 6.2 details the operation of the prescaler.

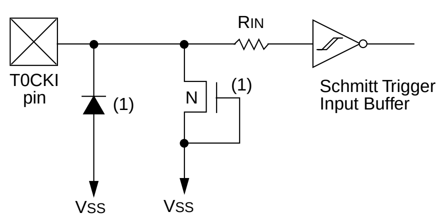
A summary of registers associated with the Timer0 module is found in Table 6-1.

FIGURE 6-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.
2: The prescaler is shared with the Watchdog Timer (Figure 6-6).

FIGURE 6-2: ELECTRICAL STRUCTURE OF T0CKI PIN



Note 1: ESD protection circuits

FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

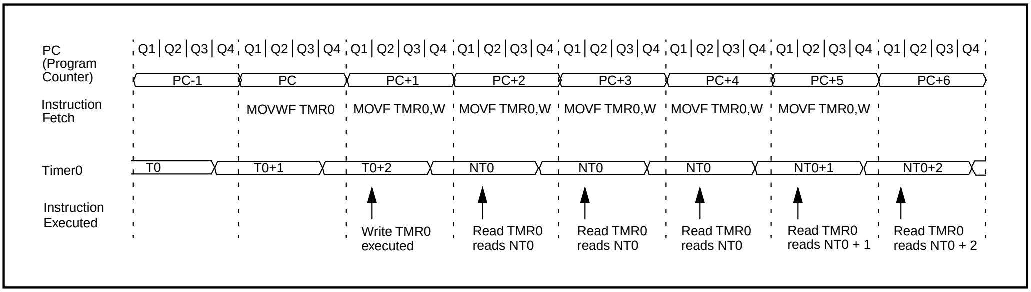


FIGURE 6-4: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

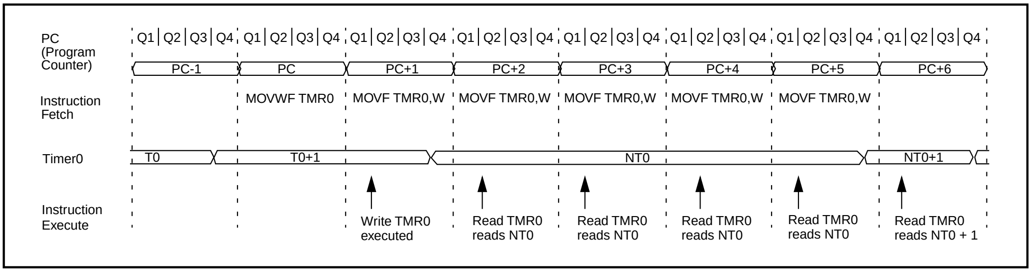


TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{MCLR}$ and WDT Reset
01h	TMR0	Timer0 - 8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
N/A	OPTION	—	—	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: Shaded cells: Unimplemented bits,
- = unimplemented, x = unknown, u = unchanged,

6.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

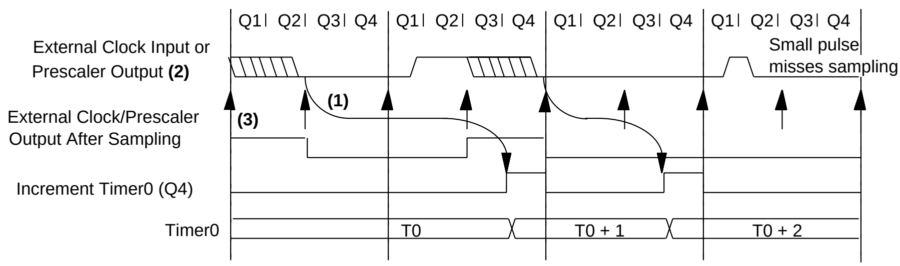
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-5). Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 6-5: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ± 4Tosc max.

2: External clock if no prescaler selected, Prescaler output otherwise.

3: The arrows indicate the points in time where sampling occurs.

6.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT) (WDT postscaler not implemented on PIC16C52), respectively (Section 6.1.2). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1, MOVWF 1, BSF 1,x,` etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

6.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

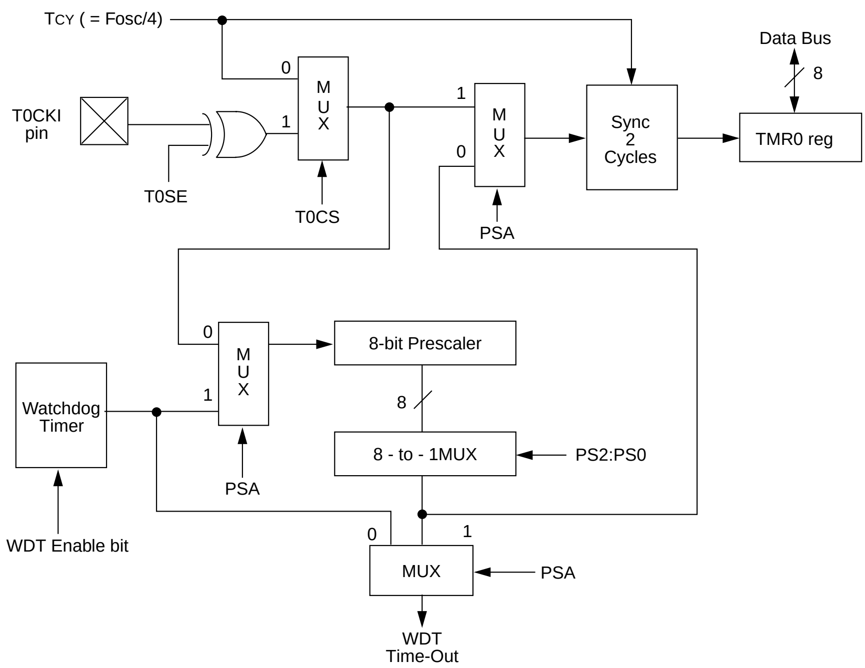
```
1.CLRWDT                ;Clear WDT
2.CLRF   TMR0           ;Clear TMR0 & Prescaler
3.MOVLW  '00xx1111'b    ;These 3 lines (5, 6, 7)
4.OPTION                ; are required only if
                        ; desired
5.CLRWDT                ;PS<2:0> are 000 or 001
6.MOVLW  '00xx1xxx'b    ;Set Postscaler to
7.OPTION                ; desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A `CLRWDT` instruction should be executed before switching the prescaler.

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                  ;Clear WDT and
                        ;prescaler
MOVLW   'xxxx0xxx'      ;Select TMR0, new
                        ;prescale value and
                        ;clock source
OPTION
```

FIGURE 6-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note: T0CS, T0SE, PSA, PS2:PS0 are bits in the OPTION register.
WDT not implemented on PIC16C52.

7.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC16C5X family of microcontrollers has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator selection
- Reset
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT)
  (not implemented on PIC16C52)
- SLEEP
- Code protection
- ID locations (not implemented on PIC16C52)

The PIC16C5X Family has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in reset until the crystal oscillator is stable. With this timer on-chip, most applications need no external reset circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake up from SLEEP through external reset or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

7.1 Configuration Bits

Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type and one bit is the Watchdog Timer enable bit. Nine bits are code protection bits (Figure 7-1 and Figure 7-2) for the PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58, and PIC16CR58 devices.

QTP or ROM devices have the oscillator configuration programmed at the factory and these parts are tested accordingly (see "Product Identification System" diagrams in the back of this data sheet).

FIGURE 7-1: CONFIGURATION WORD FOR PIC16CR54A/C54B/CR54B/C54C/CR54C/C55A/C56A/CR56A/C57C/CR57B/CR57C/C58B/CR58A/CR58B

CP	CP	CP	CP	CP	CP	CP	CP	CP	WDTE	FOSC1	FOSC0
bit11	10	9	8	7	6	5	4	3	2	1	bit0

Register: CONFIG
Address(1): FFFh

bit 11-3: **CP:** Code protection bits
1 = Code protection off
0 = Code protection on

bit 2: **WDTE:** Watchdog timer enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Refer to the PIC16C5X Programming Specification (Literature Number DS30190) to determine how to access the configuration word.

FIGURE 7-2: CONFIGURATION WORD FOR PIC16C52/C54/C54A/C55/C56/C57/C58A

—	—	—	—	—	—	—	—	CP	WDTE	FOSC1	FOSC0
bit11	10	9	8	7	6	5	4	3	2	1	bit0

Register: CONFIG
Address[1]: FFFh

bit 11-4: **Unimplemented:** Read as '0'

bit 3: **CP:** Code protection bit.
1 = Code protection off
0 = Code protection on

bit 2: **WDTE:** Watchdog timer enable bit (not implemented on PIC16C52)
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator selection bits[2]
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.
2: PIC16C52 supports XT and RC oscillator only.
PIC16LV54A supports XT, RC and LP oscillator only.
PIC16LV58A supports XT, RC and LP oscillator only.

7.2 Oscillator Configurations

7.2.1 OSCILLATOR TYPES

PIC16C5Xs can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

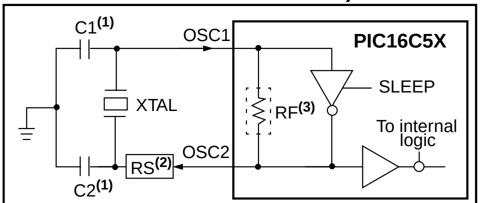
- LP: Low Power Crystal
- XT: Crystal/Resonator
- HS: High Speed Crystal/Resonator
- RC: Resistor/Capacitor

Note: Not all oscillator selections available for all parts. See Section 7.1.

7.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 7-3). The PIC16C5X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source drive the OSC1/CLKIN pin (Figure 7-4).

FIGURE 7-3: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



Note 1: See Capacitor Selection tables for recommended values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF varies with the crystal chosen (approx. value = 10 MΩ).

FIGURE 7-4: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

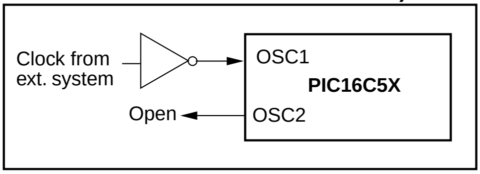


TABLE 7-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC16C5X, PIC16CR5X

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	455 kHz	22-100 pF	22-100 pF
	2.0 MHz	15-68 pF	15-68 pF
	4.0 MHz	15-68 pF	15-68 pF
HS	4.0 MHz	15-68 pF	15-68 pF
	8.0 MHz	10-68 pF	10-68 pF
	16.0 MHz	10-22 pF	10-22 pF

Note: These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 7-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC16C5X, PIC16CR5X

Osc Type	Resonator Freq	Cap.Range C1	Cap. Range C2
LP	32 kHz(1)	15 pF	15 pF
	100 kHz	15-30 pF	30-47 pF
	200 kHz	15-30 pF	15-82 pF
XT	100 kHz	15-30 pF	200-300 pF
	200 kHz	15-30 pF	100-200 pF
	455 kHz	15-30 pF	15-100 pF
	1 MHz	15-30 pF	15-30 pF
	2 MHz	15-30 pF	15-30 pF
	4 MHz	15-47 pF	15-47 pF
HS	4 MHz	15-30 pF	15-30 pF
	8 MHz	15-30 pF	15-30 pF
	20 MHz	15-30 pF	15-30 pF

Note 1: For V_{DD} > 4.5V, C1 = C2 ≈ 30 pF is recommended.
2: These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

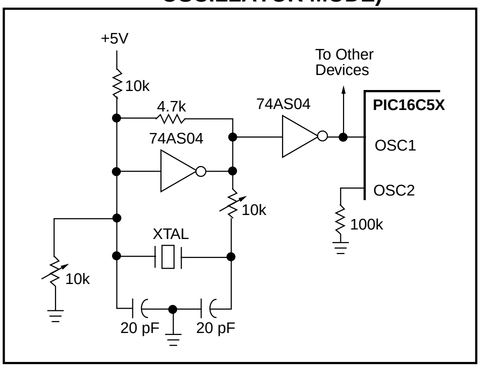
Note: If you change from this device to another device, please verify oscillator characteristics in your application.

7.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 7-5 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

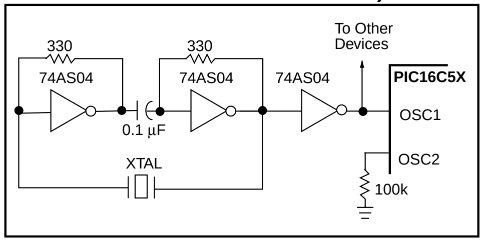
FIGURE 7-5: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)



Note:	**If you change from this device to another device, please verify oscillator characteristics in your application.**

This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 7-6: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)



Note:	**If you change from this device to another device, please verify oscillator characteristics in your application.**

7.2.4 RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 7-7 shows how the R/C combination is connected to the PIC16C5X. For Rext values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g., 1 MΩ) the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping Rext between 3 kΩ and 100 kΩ.

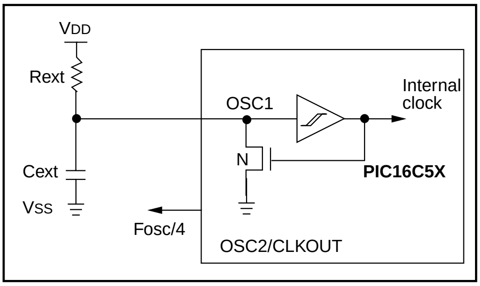
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

The Electrical Specifications sections show RC frequency variation from part to part due to normal process variation.

Also, see the Electrical Specifications sections for variation of oscillator frequency due to V_{DD} for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and V_{DD} values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic.

FIGURE 7-7: RC OSCILLATOR MODE



Note:	**If you change from this device to another device, please verify oscillator characteristics in your application.**

7.3 Reset

PIC16C5X devices may be reset in one of the following ways:

- Power-On Reset (POR)
- $\overline{\text{MCLR}}$ reset (normal operation)
- $\overline{\text{MCLR}}$ wake-up reset (from SLEEP)
- WDT reset (normal operation)
- WDT wake-up reset (from SLEEP)

Table 7-3 shows these reset conditions for the PCL and STATUS registers.

Some registers are not affected in any reset condition. Their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a “reset state” on Power-On Reset (POR), $\overline{\text{MCLR}}$ or WDT reset. A $\overline{\text{MCLR}}$ or WDT wake-up from SLEEP also results in a device reset, and not a continuation of operation before SLEEP.

The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits (STATUS <4:3>) are set or cleared depending on the different reset conditions (Section 7.7). These bits may be used to determine the nature of the reset.

Table 7-4 lists a full description of reset states of all registers. Figure 7-8 shows a simplified block diagram of the on-chip reset circuit.

TABLE 7-3: RESET CONDITIONS FOR SPECIAL REGISTERS

Condition	PCL Addr: 02h	STATUS Addr: 03h
Power-On Reset	1111 1111	0001 1xxx
$\overline{\text{MCLR}}$ reset (normal operation)	1111 1111	000u uuuu(1)
$\overline{\text{MCLR}}$ wake-up (from SLEEP)	1111 1111	0001 0uuu
WDT reset (normal operation)	1111 1111	0000 uuuu(2)
WDT wake-up (from SLEEP)	1111 1111	0000 0uuu

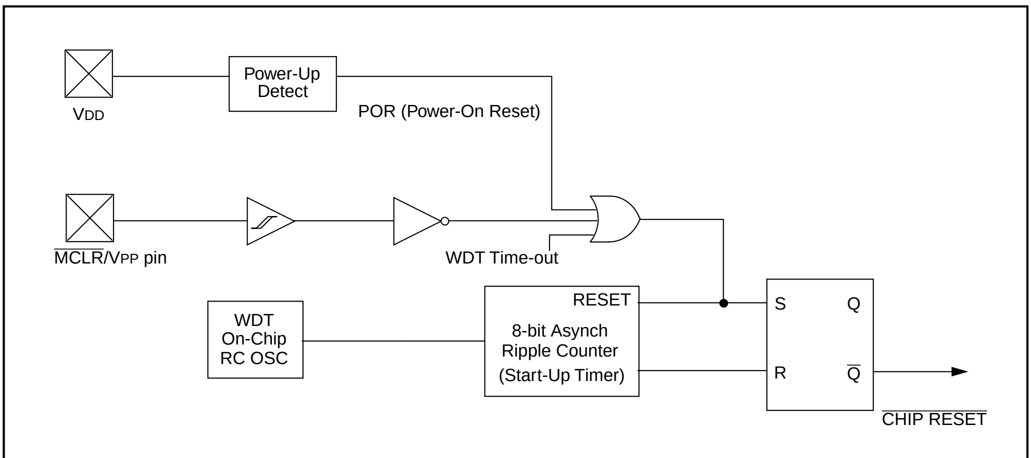
Legend: u = unchanged, x = unknown, - = unimplemented read as '0'.
Note 1: $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits retain their last value until one of the other reset conditions occur.
2: The CLRWDT instruction will set the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits.

TABLE 7-4: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-On Reset	$\overline{\text{MCLR}}$ or WDT Reset
W	N/A	xxxx xxxx	uuuu uuuu
TRIS	N/A	1111 1111	1111 1111
OPTION	N/A	--11 1111	--11 1111
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL(1)	02h	1111 1111	1111 1111
STATUS(1)	03h	0001 1xxx	000q quuu
FSR	04h	1xxx xxxx	1uuu uuuu
PORTA	05h	---- xxxx	---- uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu
PORTC(2)	07h	xxxx xxxx	uuuu uuuu
General Purpose Register Files	07-7Fh	xxxx xxxx	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented, read as '0',
q = see tables in Section 7.7 for possible values.
Note 1: See Table 7-3 for reset value for specific conditions.
2: General purpose register file on PIC16C52/C54s/CR54s/C56s/CR56s/C58s/CR58s

FIGURE 7-8: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



 Preliminary

7.4 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip reset for most power-up situations. To use this feature, the user merely ties the $\overline{MCLR}$/V_{PP} pin to V_{DD}. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 7-8.

The Power-On Reset circuit and the Device Reset Timer (Section 7.5) circuit are closely related. On power-up, the reset latch is set and the DRT is reset. The DRT timer begins counting once it detects $\overline{MCLR}$ to be high. After the time-out period, which is typically 18 ms, it will reset the reset latch and thus end the on-chip reset signal.

A power-up example where $\overline{MCLR}$ is not tied to V_{DD} is shown in Figure 7-10. V_{DD} is allowed to rise and stabilize before bringing $\overline{MCLR}$ high. The chip will actually come out of reset T_{DRT} msec after $\overline{MCLR}$ goes high.

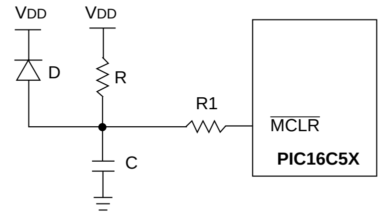
In Figure 7-11, the on-chip Power-On Reset feature is being used ($\overline{MCLR}$ and V_{DD} are tied together). The V_{DD} is stable before the start-up timer times out and there is no problem in getting a proper reset. However, Figure 7-12 depicts a problem situation where V_{DD} rises too slowly. The time between when the DRT senses a high on the $\overline{MCLR}$/V_{PP} pin, and when the $\overline{MCLR}$/V_{PP} pin (and V_{DD}) actually reach their full value, is too long. In this situation, when the start-up timer times out, V_{DD} has not reached the V_{DD} (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 7-9).

Note:	When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be meet to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the Embedded Control Handbook.

The POR circuit does not produce an internal reset when V_{DD} declines.

FIGURE 7-9: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW V_{DD} POWER-UP)



- External Power-On Reset circuit is required only if V_{DD} power-up is too slow. The diode D helps discharge the capacitor quickly when V_{DD} powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100Ω to 1 kΩ will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$ pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

FIGURE 7-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO VDD)

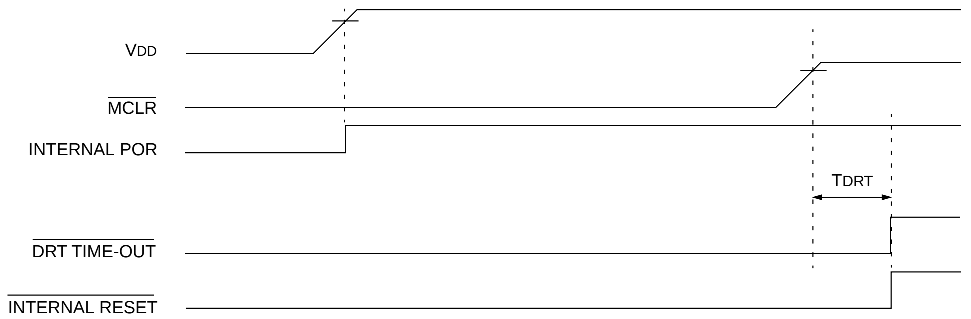


FIGURE 7-11: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO VDD): FAST VDD RISE TIME

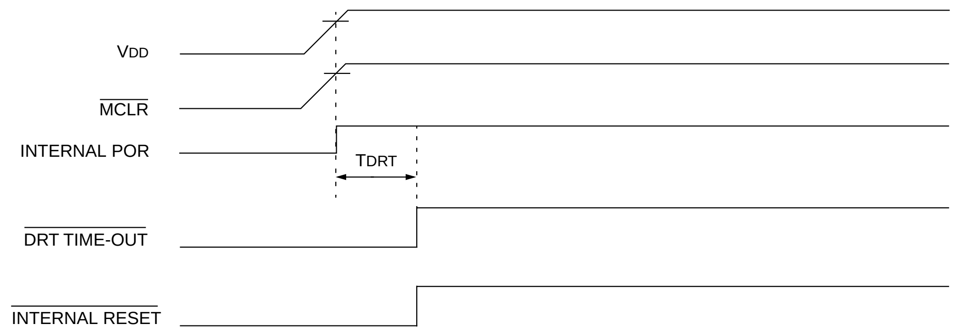
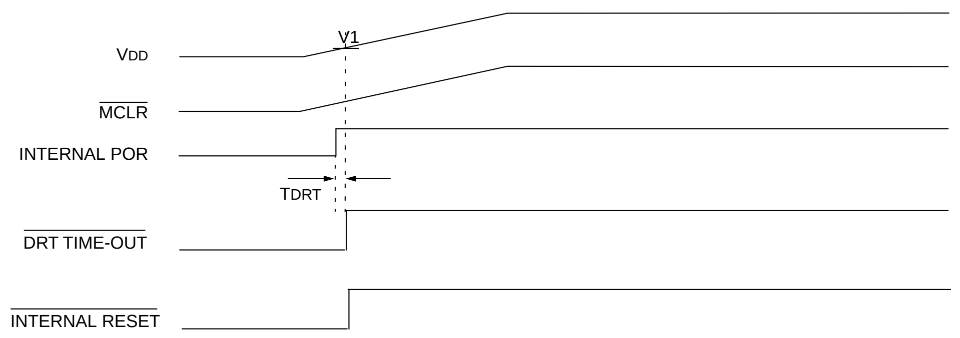


FIGURE 7-12: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO VDD): SLOW VDD RISE TIME



When VDD rises slowly, the TDRT time-out expires long before VDD has reached its final value. In this example, the chip will reset properly if, and only if, V1 ≥ VDD min

7.5 Device Reset Timer (DRT)

The Device Reset Timer (DRT) provides a fixed 18 ms nominal time-out on reset. The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows V_{DD} to rise above V_{DD} min., and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after the voltage on the $\overline{MCLR}$/V_{PP} pin has reached a logic high (V_{IH}) level. Thus, external RC networks connected to the $\overline{MCLR}$ input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The Device Reset time delay will vary from device to device due to V_{DD}, temperature, and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake the PIC16C5X from SLEEP mode automatically.

7.6 Watchdog Timer (WDT) (not implemented on PIC16C52)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT reset or wake-up reset generates a device RESET.

The $\overline{TO}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer reset.

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 7.1). Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.

7.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, V_{DD} and part-to-part process variations (see DC specs).

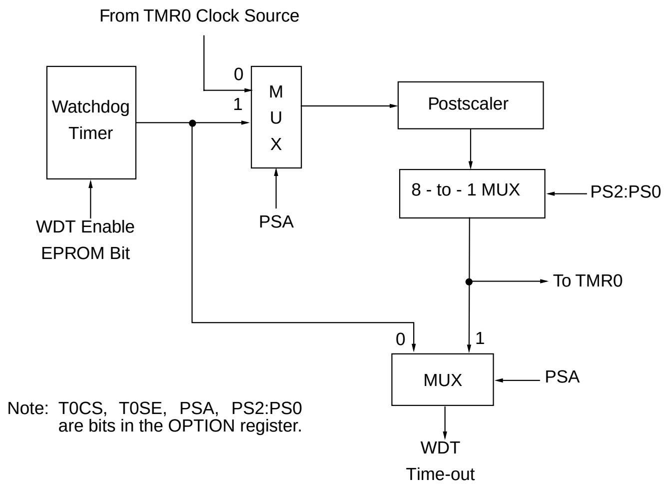
Under worst case conditions (V_{DD} = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

7.6.2 WDT PROGRAMMING CONSIDERATIONS

The `CLRWDT` instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The `SLEEP` instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT wake-up reset.

FIGURE 7-13: WATCHDOG TIMER BLOCK DIAGRAM



Note: T0CS, T0SE, PSA, PS2:PS0 are bits in the OPTION register.

TABLE 7-5: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on $\overline{MCLR}$ and WDT Reset
N/A	OPTION	—	—	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: Shaded boxes = Not used by Watchdog Timer,
– = unimplemented, read as '0', u = unchanged

7.7 Time-Out Sequence and Power Down Status Bits ($\overline{TO}$/$\overline{PD}$)

The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be tested to determine if a RESET condition has been caused by a power-up condition, a $\overline{MCLR}$ or Watchdog Timer (WDT) reset, or a $\overline{MCLR}$ or WDT wake-up reset.

TABLE 7-6: $\overline{TO}$/$\overline{PD}$ STATUS AFTER RESET

$\overline{TO}$	$\overline{PD}$	RESET was caused by
1	1	Power-up (POR)
u	u	$\overline{MCLR}$ reset (normal operation)(1)
1	0	$\overline{MCLR}$ wake-up reset (from SLEEP)
0	1	WDT reset (normal operation)
0	0	WDT wake-up reset (from SLEEP)

Legend: u = unchanged
Note 1: The $\overline{TO}$ and $\overline{PD}$ bits maintain their status (u) until a reset occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{TO}$ and $\overline{PD}$ status bits.

These STATUS bits are only affected by events listed in Table 7-7.

TABLE 7-7: EVENTS AFFECTING $\overline{TO}$/$\overline{PD}$ STATUS BITS

Event	$\overline{TO}$	$\overline{PD}$	Remarks
Power-up	1	1	
WDT Time-out	0	u	No effect on $\overline{PD}$
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

Legend: u = unchanged

Note: A WDT time-out will occur regardless of the status of the $\overline{TO}$ bit. A SLEEP instruction will be executed, regardless of the status of the $\overline{PD}$ bit.

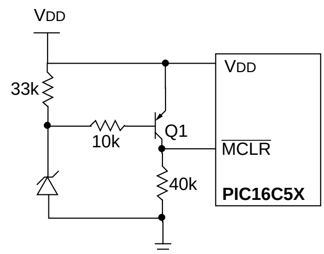
Table 7-3 lists the reset conditions for the special function registers, while Table 7-4 lists the reset conditions for all the registers.

7.8 Reset on Brown-Out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

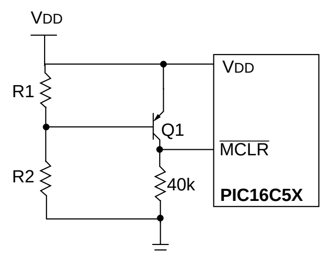
To reset PIC16C5X devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 7-14 and Figure 7-15.

FIGURE 7-14: BROWN-OUT PROTECTION CIRCUIT 1



This circuit will activate reset when VDD goes below Vz + 0.7V (where Vz = Zener voltage).

FIGURE 7-15: BROWN-OUT PROTECTION CIRCUIT 2



This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7V$$

7.9 Power-Down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

7.9.1 SLEEP

The Power-Down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the $\overline{MCLR}/V_{PP}$ pin low.

For lowest current consumption while powered down, the T0CKI input should be at V_{DD} or V_{SS} and the $\overline{MCLR}/V_{PP}$ pin must be at a logic high level.

7.9.2 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. An external reset input on $\overline{MCLR}/V_{PP}$ pin.
2. A Watchdog Timer time-out reset (if WDT was enabled).

Both of these events cause a device reset. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the cause of device reset. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked.

The WDT is cleared when the device wakes from sleep, regardless of the wake-up source.

7.10 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note:	Microchip does not recommend code protecting windowed devices.

7.11 ID Locations (not implemented on PIC16C52)

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

Note:	Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code.

8.0 INSTRUCTION SET SUMMARY

Each PIC16C5X instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type, and one or more operands which further specify the operation of the instruction. The PIC16C5X instruction set summary in Table 8-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 8-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 8-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
$\overline{TO}$	Time-Out bit
$\overline{PD}$	Power-Down bit
dest	Destination, either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term (font is courier)

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µs.

Figure 8-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 8-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations

11 6	5	4 0
OPCODE	d	f (FILE #)

d = 0 for destination W
d = 1 for destination f
f = 5-bit file register address

Bit-oriented file register operations

11 8	7 5	4 0
OPCODE	b (BIT #)	f (FILE #)

b = 3-bit bit address
f = 5-bit file register address

Literal and control operations (except GOTO)

11 8	7 0
OPCODE	k (literal)

k = 8-bit immediate value

Literal and control operations - GOTO instruction

11 9	8 0
OPCODE	k (literal)

k = 9-bit immediate value

TABLE 8-2: INSTRUCTION SET SUMMARY

Mnemonic,	Operands	Description	Cycles	12-Bit Opcode MSb		LSb	Status Affected	Notes
ADDWF	f,d	Add W and f	1	0001	11df	ffff	C,DC,Z	1,2,4
ANDWF	f,d	AND W with f	1	0001	01df	ffff	Z	2,4
CLRF	f	Clear f	1	0000	011f	ffff	Z	4
CLRW	–	Clear W	1	0000	0100	0000	Z	
COMF	f, d	Complement f	1	0010	01df	ffff	Z	
DECF	f, d	Decrement f	1	0000	11df	ffff	Z	2,4
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	0010	11df	ffff	None	2,4
INCF	f, d	Increment f	1	0010	10df	ffff	Z	2,4
INCFSZ	f, d	Increment f, Skip if 0	1(2)	0011	11df	ffff	None	2,4
IORWF	f, d	Inclusive OR W with f	1	0001	00df	ffff	Z	2,4
MOVF	f, d	Move f	1	0010	00df	ffff	Z	2,4
MOVWF	f	Move W to f	1	0000	001f	ffff	None	1,4
NOP	–	No Operation	1	0000	0000	0000	None	
RLF	f, d	Rotate left f through Carry	1	0011	01df	ffff	C	2,4
RRF	f, d	Rotate right f through Carry	1	0011	00df	ffff	C	2,4
SUBWF	f, d	Subtract W from f	1	0000	10df	ffff	C,DC,Z	1,2,4
SWAPF	f, d	Swap f	1	0011	10df	ffff	None	2,4
XORWF	f, d	Exclusive OR W with f	1	0001	10df	ffff	Z	2,4
BIT-ORIENTED FILE REGISTER OPERATIONS								
BCF	f, b	Bit Clear f	1	0100	bbbf	ffff	None	2,4
BSF	f, b	Bit Set f	1	0101	bbbf	ffff	None	2,4
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	0110	bbbf	ffff	None	
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	0111	bbbf	ffff	None	
LITERAL AND CONTROL OPERATIONS								
ANDLW	k	AND literal with W	1	1110	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	1001	kkkk	kkkk	None	1
CLRWDT	k	Clear Watchdog Timer	1	0000	0000	0100	$\overline{TO}$, $\overline{PD}$	
GOTO	k	Unconditional branch	2	101k	kkkk	kkkk	None	
IORLW	k	Inclusive OR Literal with W	1	1101	kkkk	kkkk	Z	
MOVLW	k	Move Literal to W	1	1100	kkkk	kkkk	None	
OPTION	k	Load OPTION register	1	0000	0000	0010	None	
RETLW	k	Return, place Literal in W	2	1000	kkkk	kkkk	None	
SLEEP	–	Go into standby mode	1	0000	0000	0011	$\overline{TO}$, $\overline{PD}$	
TRIS	f	Load TRIS register	1	0000	0000	0fff	None	3
XORLW	k	Exclusive OR Literal to W	1	1111	kkkk	kkkk	Z	

Note 1: The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for `GOTO`. (See individual device data sheets, Memory Section/Indirect Data Addressing, INDF and FSR Registers)

2: When an I/O register is modified as a function of itself (e.g. `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

3: The instruction `TRIS f`, where f = 5 or 6 causes the contents of the W register to be written to the tristate latches of PORTA or B respectively. A '1' forces the pin to a hi-impedance state and disables the output buff-ers.

4: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).

ADDWF **Add W and f**

Syntax: [*label*] ADDWF f,d

Operands: $0 \le f \le 31$
d ∈ [0,1]

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Encoding:

`0001`	`11df`	`ffff`

Description: Add the contents of the W register and register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: `ADDWF FSR, 0`

Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0xD9
FSR = 0xC2

ANDWF **AND W with f**

Syntax: [*label*] ANDWF f,d

Operands: $0 \le f \le 31$
d ∈ [0,1]

Operation: (W) .AND. (f) → (dest)

Status Affected: Z

Encoding:

`0001`	`01df`	`ffff`

Description: The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: `ANDWF FSR, 1`

Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0x17
FSR = 0x02

ANDLW **And literal with W**

Syntax: [*label*] ANDLW k

Operands: $0 \le k \le 255$

Operation: (W).AND. (k) → (W)

Status Affected: Z

Encoding:

`1110`	`kkkk`	`kkkk`

Description: The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: `ANDLW 0x5F`

Before Instruction
W = 0xA3

After Instruction
W = 0x03

BCF **Bit Clear f**

Syntax: [*label*] BCF f,b

Operands: $0 \le f \le 31$
$0 \le b \le 7$

Operation: 0 → (f<b>)

Status Affected: None

Encoding:

`0100`	`bbbf`	`ffff`

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example: `BCF FLAG_REG, 7`

Before Instruction
FLAG_REG = 0xC7

After Instruction
FLAG_REG = 0x47

BSF — Bit Set f

Syntax:	[*label*] BSF f,b
Operands:	0 ≤ f ≤ 31 0 ≤ b ≤ 7
Operation:	1 → (f<b>)
Status Affected:	None
Encoding:	`0101` | `bbbf` | `ffff`
Description:	Bit 'b' in register 'f' is set.
Words:	1
Cycles:	1
Example:	`BSF FLAG_REG, 7`

Before Instruction
FLAG_REG = 0x0A

After Instruction
FLAG_REG = 0x8A

BTFSC — Bit Test f, Skip if Clear

Syntax:	[*label*] BTFSC f,b
Operands:	0 ≤ f ≤ 31 0 ≤ b ≤ 7
Operation:	skip if (f<b>) = 0
Status Affected:	None
Encoding:	`0110` | `bbbf` | `ffff`
Description:	If bit 'b' in register 'f' is 0 then the next instruction is skipped. If bit 'b' is 0 then the next instruction fetched during the current instruction execution is discarded, and an NOP is executed instead, making this a 2 cycle instruction.
Words:	1
Cycles:	1(2)

Example:

```
HERE    BTFSC  FLAG,1
FALSE   GOTO   PROCESS_CODE
TRUE    •
        •
        •
```

Before Instruction
PC = address (HERE)

After Instruction
if FLAG<1> = 0,
PC = address (TRUE);
if FLAG<1> = 1,
PC = address(FALSE)

BTFSS — Bit Test f, Skip if Set

Syntax:	[*label*] BTFSS f,b
Operands:	0 ≤ f ≤ 31 0 ≤ b < 7
Operation:	skip if (f<b>) = 1
Status Affected:	None
Encoding:	`0111` | `bbbf` | `ffff`
Description:	If bit 'b' in register 'f' is '1' then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and an NOP is executed instead, making this a 2 cycle instruction.
Words:	1
Cycles:	1(2)

Example:

```
HERE    BTFSS  FLAG,1
FALSE   GOTO   PROCESS_CODE
TRUE    •
        •
        •
```

Before Instruction
PC = address (HERE)

After Instruction
If FLAG<1> = 0,
PC = address (FALSE);
if FLAG<1> = 1,
PC = address (TRUE)

CALL — Subroutine Call

Syntax: [*label*] CALL k

Operands: 0 ≤ k ≤ 255

Operation: (PC) + 1→ Top of Stack;
k → PC<7:0>;
(STATUS<6:5>) → PC<10:9>;
0 → PC<8>

Status Affected: None

Encoding:

1001	kkkk	kkkk

Description: Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. `CALL` is a two cycle instruction.

Words: 1

Cycles: 2

Example: `HERE CALL THERE`

Before Instruction
PC = address (`HERE`)

After Instruction
PC = address (`THERE`)
TOS = address (`HERE + 1`)

CLRF — Clear f

Syntax: [*label*] CLRF f

Operands: 0 ≤ f ≤ 31

Operation: 00h → (f);
1 → Z

Status Affected: Z

Encoding:

0000	011f	ffff

Description: The contents of register 'f' are cleared and the Z bit is set.

Words: 1

Cycles: 1

Example: `CLRF FLAG_REG`

Before Instruction
FLAG_REG = 0x5A

After Instruction
FLAG_REG = 0x00
Z = 1

CLRW — Clear W

Syntax: [*label*] CLRW

Operands: None

Operation: 00h → (W);
1 → Z

Status Affected: Z

Encoding:

0000	0100	0000

Description: The W register is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example: `CLRW`

Before Instruction
W = 0x5A

After Instruction
W = 0x00
Z = 1

CLRWDT — Clear Watchdog Timer

Syntax: [*label*] CLRWDT

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler (if assigned);
1 → $\overline{TO}$;
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

0000	0000	0100

Description: The `CLRWDT` instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

Example: `CLRWDT`

Before Instruction
WDT counter = ?

After Instruction
WDT counter = 0x00
WDT prescale = 0
$\overline{TO}$ = 1
$\overline{PD}$ = 1

COMF **Complement f**

Syntax: [*label*] COMF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

Operation: $(\bar{f}) \rightarrow$ (dest)

Status Affected: Z

Encoding:

`0010`	`01df`	`ffff`

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: `COMF REG1,0`

Before Instruction
REG1 = 0x13

After Instruction
REG1 = 0x13
W = 0xEC

DECF **Decrement f**

Syntax: [*label*] DECF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

Operation: (f) – 1 → (dest)

Status Affected: Z

Encoding:

`0000`	`11df`	`ffff`

Description: Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: `DECF CNT, 1`

Before Instruction
CNT = 0x01
Z = 0

After Instruction
CNT = 0x00
Z = 1

DECFSZ **Decrement f, Skip if 0**

Syntax: [*label*] DECFSZ f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

Operation: (f) – 1 → d; skip if result = 0

Status Affected: None

Encoding:

`0010`	`11df`	`ffff`

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

If the result is 0, the next instruction, which is already fetched, is discarded and an NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1(2)

Example:

```
HERE      DECFSZ   CNT, 1
          GOTO     LOOP
CONTINUE  •
          •
          •
```

Before Instruction
PC = address `(HERE)`

After Instruction
CNT = CNT - 1;
if CNT = 0,
PC = address `(CONTINUE)`;
if CNT ≠ 0,
PC = address `(HERE+1)`

GOTO **Unconditional Branch**

Syntax: [*label*] GOTO k

Operands: 0 ≤ k ≤ 511

Operation: k → PC<8:0>;
STATUS<6:5> → PC<10:9>

Status Affected: None

Encoding:

`101k`	`kkkk`	`kkkk`

Description: `GOTO` is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. `GOTO` is a two cycle instruction.

Words: 1

Cycles: 2

Example: `GOTO THERE`

After Instruction
PC = address `(THERE)`

INCF — Increment f

Syntax: [*label*] INCF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

Operation: (f) + 1 → (dest)

Status Affected: Z

Encoding:

`0010`	`10df`	`ffff`

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example: `INCF CNT, 1`

Before Instruction
CNT = 0xFF
Z = 0

After Instruction
CNT = 0x00
Z = 1

INCFSZ — Increment f, Skip if 0

Syntax: [*label*] INCFSZ f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

Operation: (f) + 1 → (dest), skip if result = 0

Status Affected: None

Encoding:

`0011`	`11df`	`ffff`

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

If the result is 0, then the next instruction, which is already fetched, is discarded and an NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1(2)

Example:

```
HERE      INCFSZ    CNT,  1
          GOTO     LOOP
CONTINUE  •
          •
          •
```

Before Instruction
PC = address (HERE)

After Instruction
CNT = CNT + 1;
if CNT = 0,
PC = address (CONTINUE);
if CNT ≠ 0,
PC = address (HERE +1)

IORLW — Inclusive OR literal with W

Syntax: [*label*] IORLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) .OR. (k) → (W)

Status Affected: Z

Encoding:

`1101`	`kkkk`	`kkkk`

Description: The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: `IORLW 0x35`

Before Instruction
W = 0x9A

After Instruction
W = 0xBF
Z = 0

IORWF — Inclusive OR W with f

Syntax: [*label*] IORWF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

Operation: (W).OR. (f) → (dest)

Status Affected: Z

Encoding:

`0001`	`00df`	`ffff`

Description: Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example: `IORWF RESULT, 0`

Before Instruction
RESULT = 0x13
W = 0x91

After Instruction
RESULT = 0x13
W = 0x93
Z = 0

MOVF — Move f

Syntax:	[*label*] MOVF f,d
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operation:	(f) → (dest)
Status Affected:	Z
Encoding:	`0010` `00df` `ffff`
Description:	The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.
Words:	1
Cycles:	1
Example:	`MOVF FSR, 0`

After Instruction
W = value in FSR register

MOVLW — Move Literal to W

Syntax:	[*label*] MOVLW k
Operands:	$0 \le k \le 255$
Operation:	k → (W)
Status Affected:	None
Encoding:	`1100` `kkkk` `kkkk`
Description:	The eight bit literal 'k' is loaded into the W register. The don't cares will assemble as 0s.
Words:	1
Cycles:	1
Example:	`MOVLW 0x5A`

After Instruction
W = 0x5A

MOVWF — Move W to f

Syntax:	[*label*] MOVWF f
Operands:	$0 \le f \le 31$
Operation:	(W) → (f)
Status Affected:	None
Encoding:	`0000` `001f` `ffff`
Description:	Move data from the W register to register 'f'.
Words:	1
Cycles:	1
Example:	`MOVWF TEMP_REG`

Before Instruction
TEMP_REG = 0xFF
W = 0x4F

After Instruction
TEMP_REG = 0x4F
W = 0x4F

NOP — No Operation

Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Encoding:	`0000` `0000` `0000`
Description:	No operation.
Words:	1
Cycles:	1
Example:	`NOP`

OPTION — Load OPTION Register

Syntax: [*label*] OPTION

Operands: None

Operation: (W) → OPTION

Status Affected: None

Encoding:

0000	0000	0010

Description: The content of the W register is loaded into the OPTION register.

Words: 1

Cycles: 1

Example `OPTION`

Before Instruction
W = 0x07

After Instruction
OPTION = 0x07

RETLW — Return with Literal in W

Syntax: [*label*] RETLW k

Operands: 0 ≤ k ≤ 255

Operation: k → (W);
TOS → PC

Status Affected: None

Encoding:

1000	kkkk	kkkk

Description: The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

Words: 1

Cycles: 2

Example:

```
        CALL TABLE ;W contains
                   ;table offset
                   ;value.
        •          ;W now has table
        •          ;value.
        •
TABLE   ADDWF PC   ;W = offset
        RETLW k1   ;Begin table
        RETLW k2   ;
        •
        •
        •
        RETLW kn   ; End of table
```

Before Instruction
W = 0x07

After Instruction
W = value of k8

RLF — Rotate Left f through Carry

Syntax: [*label*] RLF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

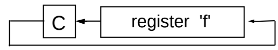
Operation: See description below

Status Affected: C

Encoding:

0011	01df	ffff

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example: `RLF REG1,0`

Before Instruction
REG1 = 1110 0110
C = 0

After Instruction
REG1 = 1110 0110
W = 1100 1100
C = 1

RRF — Rotate Right f through Carry

Syntax: [*label*] RRF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

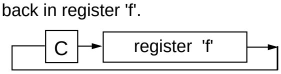
Operation: See description below

Status Affected: C

Encoding:

0011	00df	ffff

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.



Words: 1

Cycles: 1

Example: `RRF REG1,0`

Before Instruction
REG1 = 1110 0110
C = 0

After Instruction
REG1 = 1110 0110
W = 0111 0011
C = 0

SLEEP — Enter SLEEP Mode

Syntax:	[*label*] SLEEP
Operands:	None
Operation:	00h → WDT; 0 → WDT prescaler; 1 → $\overline{TO}$; 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Encoding:	`0000` `0000` `0011`
Description:	Time-out status bit ($\overline{TO}$) is set. The power down status bit ($\overline{PD}$) is cleared. The WDT and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.
Words:	1
Cycles:	1
Example:	SLEEP

SUBWF — Subtract W from f

Syntax:	[*label*] SUBWF f,d
Operands:	0 ≤ f ≤ 31 d ∈ [0,1]
Operation:	(f) – (W) → (dest)
Status Affected:	C, DC, Z
Encoding:	`0000` `10df` `ffff`
Description:	Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example 1:	`SUBWF REG1, 1`

Before Instruction
REG1 = 3
W = 2
C = ?

After Instruction
REG1 = 1
W = 2
C = 1 ; result is positive

Example 2:

Before Instruction
REG1 = 2
W = 2
C = ?

After Instruction
REG1 = 0
W = 2
C = 1 ; result is zero

Example 3:

Before Instruction
REG1 = 1
W = 2
C = ?

After Instruction
REG1 = FF
W = 2
C = 0 ; result is negative

SWAPF — Swap Nibbles in f

Syntax: [*label*] SWAPF f,d

Operands: $0 \leq f \leq 31$
$d \in [0,1]$

Operation: (f<3:0>) → (dest<7:4>);
(f<7:4>) → (dest<3:0>)

Status Affected: None

Encoding:

`0011`	`10df`	`ffff`

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Example `SWAPF REG1, 0`

Before Instruction
REG1 = 0xA5

After Instruction
REG1 = 0xA5
W = 0X5A

TRIS — Load TRIS Register

Syntax: [*label*] TRIS f

Operands: f = 5, 6 or 7

Operation: (W) → TRIS register f

Status Affected: None

Encoding:

`0000`	`0000`	`0fff`

Description: TRIS register 'f' (f = 5, 6, or 7) is loaded with the contents of the W register

Words: 1

Cycles: 1

Example `TRIS PORTA`

Before Instruction
W = 0XA5

After Instruction
TRISA = 0XA5

XORLW — Exclusive OR literal with W

Syntax: [*label*] XORLW k

Operands: $0 \leq k \leq 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

`1111`	`kkkk`	`kkkk`

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: `XORLW 0xAF`

Before Instruction
W = 0xB5

After Instruction
W = 0x1A

XORWF — Exclusive OR W with f

Syntax: [*label*] XORWF f,d

Operands: $0 \leq f \leq 31$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (dest)

Status Affected: Z

Encoding:

`0001`	`10df`	`ffff`

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example `XORWF REG,1`

Before Instruction
REG = 0xAF
W = 0xB5

After Instruction
REG = 0x1A
W = 0xB5

NOTES:

9.0 DEVELOPMENT SUPPORT

9.1 Development Tools

The PICmicro™ microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER®/PICMASTER CE Real-Time In-Circuit Emulator
- ICEPIC™ Low-Cost PIC16C5X and PIC16CXXX In-Circuit Emulator
- PRO MATE® II Universal Programmer
- PICSTART® Plus Entry-Level Prototype Programmer
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB™ SIM Software Simulator
- MPLAB-C17 (C Compiler)
- Fuzzy Logic Development System (*fuzzy*TECH®–MP)

9.2 PICMASTER: High Performance Universal In-Circuit Emulator with MPLAB IDE

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC14C000, PIC12CXXX, PIC16C5X, PIC16CXXX and PIC17CXX families. PICMASTER is supplied with the MPLAB™ Integrated Development Environment (IDE), which allows editing, “make” and download, and source debugging from a single environment.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new Microchip microcontrollers.

The PICMASTER Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows® 3.x environment were chosen to best make these features available to you, the end user.

A CE compliant version of PICMASTER is available for European Union (EU) countries.

9.3 ICEPIC: Low-Cost PICmicro™ In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC12CXXX, PIC16C5X and PIC16CXXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 286-AT® through Pentium™ based machines under Windows 3.x environment. ICEPIC features real time, non-intrusive emulation.

9.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode. PRO MATE II is CE compliant.

The PRO MATE II has programmable V_{DD} and V_{PP} supplies which allows it to verify programmed memory at V_{DD} min and V_{DD} max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode the PRO MATE II can read, verify or program PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices. It can also set configuration and code-protect bits in this mode.

9.5 PICSTART Plus Entry Level Development System

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923, PIC16C924 and PIC17C756 may be supported with an adapter socket. PICSTART Plus is CE compliant.

9.6 PICDEM-1 Low-Cost PICmicro Demonstration Board

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-Plus programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the PICMASTER emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

9.7 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-Plus, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I^2C bus and separate headers for connection to an LCD module and a keypad.

9.8 PICDEM-3 Low-Cost PIC16CXXX Demonstration Board

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

9.9 MPLAB™ Integrated Development Environment Software

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- A full featured editor
- Three operating modes
  - editor
  - emulator
  - simulator
- A project manager
- Customizable tool bar and key mapping
- A status bar with project information
- Extensive on-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PICmicro tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
- Transfer data dynamically via DDE (soon to be replaced by OLE)
- Run up to four emulators on the same PC

The ability to use MPLAB with Microchip's simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

9.10 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PC-hosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from PICMASTER, Microchip's Universal Emulator System.

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro assembly capability.
- Produces all the files (Object, Listing, Symbol, and special) required for symbolic debug with Microchip's emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a rich directive language to support programming of the PICmicro. Directives are helpful in making the development of your assemble source code shorter and more maintainable.

9.11 Software Simulator (MPLAB-SIM)

The MPLAB-SIM Software Simulator allows code development in a PC host environment. It allows the user to simulate the PICmicro series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in; single step, execute until break, or in a trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C and MPASM. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

9.12 C Compiler (MPLAB-C17)

The MPLAB-C Code Development System is a complete 'C' compiler and integrated development environment for Microchip's PIC17CXXX family of microcontrollers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the MPLAB IDE memory display.

9.13 Fuzzy Logic Development System (*fuzzy*TECH-MP)

*fuzzy*TECH-MP fuzzy logic development tool is available in two versions - a low cost introductory version, MP Explorer, for designers to gain a comprehensive working knowledge of fuzzy logic system design; and a full-featured version, *fuzzy*TECH-MP, Edition for implementing more complex systems.

Both versions include Microchip's *fuzzy*LAB™ demonstration board for hands-on experience with fuzzy logic systems implementation.

9.14 MP-DriveWay™ – Application Code Generator

MP-DriveWay is an easy-to-use Windows-based Application Code Generator. With MP-DriveWay you can visually configure all the peripherals in a PICmicro device and, with a click of the mouse, generate all the initialization and many functional code modules in C language. The output is fully compatible with Microchip's MPLAB-C C compiler. The code produced is highly modular and allows easy integration of your own code. MP-DriveWay is intelligent enough to maintain your code through subsequent code generation.

9.15 SEEVAL® Evaluation and Programming System

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials™ and secure serials. The Total Endurance™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

9.16 KEELOQ® Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

TABLE 9-1: DEVELOPMENT TOOLS FROM MICROCHIP

	PIC12C5XX	PIC14000	PIC16C5X	PIC16CXXX	PIC16C6X	PIC16C7XX	PIC16C8X	PIC16C9XX	PIC17C4X	PIC17C7XX	24CXX 25CXX 93CXX	HCSXXX
EMULATOR PRODUCTS												
PICMASTER®/ PICMASTER-CE In-Circuit Emulator	✓	✓	✓	✓	✓	✓	✓	✓	✓	(PIC17C75X only) ✓		
MPLAB™-ICE										✓		
ICEPIC™ Low-Cost In-Circuit Emulator	✓		✓	✓	✓	✓	✓	✓				
SOFTWARE PRODUCTS												
MPLAB™ Integrated Development Environment	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
MPLAB™ C17 Compiler									✓	✓		
***fuzzy*TECH®-MP Explorer/Edition Fuzzy Logic Dev. Tool**	✓	✓	✓	✓	✓	✓	✓	✓	✓			
MP-DriveWay™ Applications Code Generator			✓	✓	✓	✓	✓	✓	✓			
Total Endurance™ Software Model											✓	
PROGRAMMERS												
PICSTART®Plus Low-Cost Universal Dev. Kit	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
PRO MATE® II Universal Programmer	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
KEELOQ® Programmer												✓
DEMO BOARDS												
SEEVAL® Designers Kit											✓	
PICDEM-1			✓	✓			✓		✓			
PICDEM-2					✓	✓						
PICDEM-3								✓				
KEELOQ® Evaluation Kit												✓

Preliminary

10.0 ELECTRICAL CHARACTERISTICS - PIC16C52

Absolute Maximum Ratings†

Ambient Temperature under bias .... –55°C to +125°C
Storage Temperature .... –65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} .... 0 V to +7.5 V
Voltage on $\overline{MCLR}$ with respect to V_{SS} .... 0 V to +14 V
Voltage on all other pins with respect to V_{SS} .... –0.6 V to (V_{DD} + 0.6 V)
Total Power Dissipation(1) .... 800 mW
Max. Current out of V_{SS} pin .... 150 mA
Max. Current into V_{DD} pin .... 50 mA
Max. Current into an input pin (T0CKI only) .... ±500 μA
Input Clamp Current, I_{IK} (V_I < 0 or V_I > V_{DD}) .... ±20 mA
Output Clamp Current, I_{OK} (V_O < 0 or V_O > V_{DD}) .... ±20 mA
Max. Output Current sunk by any I/O pin .... 10 mA
Max. Output Current sourced by any I/O pin .... 10 mA
Max. Output Current sourced by a single I/O port (PORTA or B) .... 10 mA
Max. Output Current sunk by a single I/O port (PORTA or B) .... 10 mA

Note 1: Power Dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

10.1 DC Characteristics: PIC16C52-04 (Commercial) PIC16C52-04I (Industrial)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	3.0	—	6.25	V	FOSC = DC to 4 MHz
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP Mode
Supply Current(3,4)	IDD	—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5 V
Power Down Current(5)	IPD	—				
Commercial			0.6	9	μA	VDD = 3.0 V
Industrial			0.6	12	μA	VDD = 3.0 V

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: For RC option, does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

Preliminary

10.2 DC Characteristics: PIC16C52-04 (Commercial) PIC16C52-04I (Industrial)

DC Characteristics All Pins Except Power Supply Pins	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature $0°C \le T_A \le +70°C$ (commercial) $-40°C \le T_A \le +85°C$ (industrial) Operating Voltage V_{DD} range is described in Section 10.1.					
Characteristic	**Sym**	**Min**	**Typ[1]**	**Max**	**Units**	**Conditions**
Input Low Voltage	V_{IL}		—			
I/O ports		V_{SS}	—	0.2 V_{DD}	V	Pin at hi-impedance
$\overline{MCLR}$ (Schmitt Trigger)		V_{SS}	—	0.15 V_{DD}	V	
T0CKI (Schmitt Trigger)		V_{SS}	—	0.15 V_{DD}	V	
OSC1 (Schmitt Trigger)		V_{SS}	—	0.15 V_{DD}	V	RC[4] option only
		V_{SS}	—	0.3 V_{DD}	V	XT option
Input High Voltage	V_{IH}		—			
I/O ports		0.45 V_{DD}	—	V_{DD}	V	For all V_{DD}[5]
		2.0	—	V_{DD}	V	4.0 V < V_{DD} ≤ 5.5 V[5]
		0.36 V_{DD}	—	V_{DD}	V	V_{DD} > 5.5 V
$\overline{MCLR}$ (Schmitt Trigger)		0.85 V_{DD}	—	V_{DD}	V	
T0CKI (Schmitt Trigger)		0.85 V_{DD}	—	V_{DD}	V	
OSC1 (Schmitt Trigger)		0.85 V_{DD}	—	V_{DD}	V	RC[4] option only
		0.7 V_{DD}	—	V_{DD}	V	XT option
Hysteresis of Schmitt Trigger inputs	V_{HYS}	0.15V_{DD}*	—	—	V	
Input Leakage Current[2,3]	I_{IL}					**For V_{DD} ≤ 5.5 V**
I/O ports		–1	0.5	+1	µA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at hi-impedance
$\overline{MCLR}$		–5			µA	$V_{PIN} = V_{SS} + 0.25$ V
			0.5	+5	µA	$V_{PIN} = V_{DD}$
T0CKI		–3	0.5	+3	µA	$V_{SS} \le V_{PIN} \le V_{DD}$
OSC1		–3	0.5	+3	µA	$V_{SS} \le V_{PIN} \le V_{DD}$, XT option
Output Low Voltage	V_{OL}	—	—			
I/O ports		—	—	0.6	V	I_{OL} = 2.0 mA, V_{DD} = 4.5 V
OSC2/CLKOUT		—	—	0.6	V	I_{OL} = 1.6 mA, V_{DD} = 4.5 V, RC option
Output High Voltage	V_{OH}		—	—		
I/O ports[3]		V_{DD} – 0.7	—	—	V	I_{OH} = –2.0 mA, V_{DD} = 4.5 V
OSC2/CLKOUT		V_{DD} – 0.7	—	—	V	I_{OH} = –1.0 mA, V_{DD} = 4.5 V, RC option

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the $\overline{MCLR}$/V_{PP} pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C52 be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

10.3 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

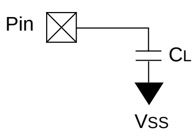
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port		

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 10-1: LOAD CONDITIONS - PIC16C52



C_L = 50 pF for all pins except OSC2

15 pF for OSC2 in XT mode when external clock is used to drive OSC1

10.4 Timing Diagrams and Specifications

FIGURE 10-2: EXTERNAL CLOCK TIMING - PIC16C52

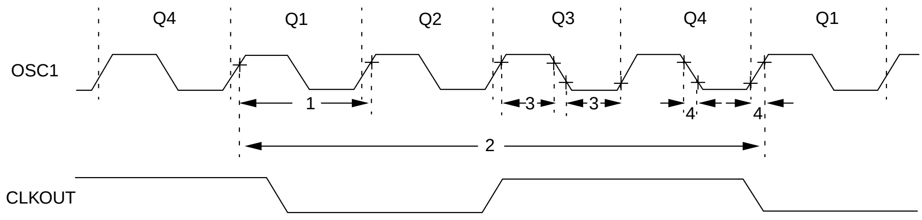


TABLE 10-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C52

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 10.1.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	FOSC	External CLKIN Frequency(2)	DC	—	4	MHz	XT osc mode
		Oscillator Frequency(2)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
1	TOSC	External CLKIN Period(2)	250	—	—	ns	RC osc mode
			250	—	—	ns	XT osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	—	—	ns	XT oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator

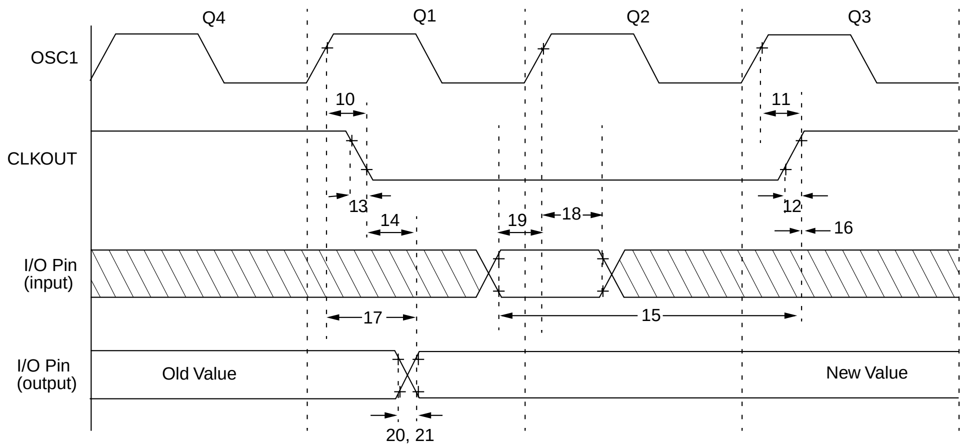
* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 10-3: CLKOUT AND I/O TIMING - PIC16C52



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

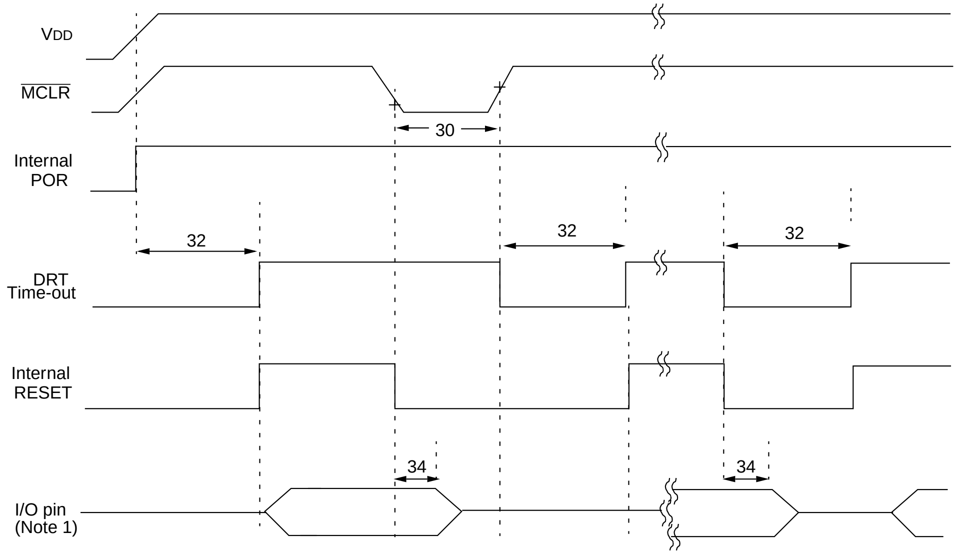
TABLE 10-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C52

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 10.1.					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5	15**	ns
13	TckF	CLKOUT fall time(2)	—	5	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.
** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.
3: See Figure 10-1 for loading conditions.

FIGURE 10-4: RESET AND DEVICE RESET TIMER TIMING - PIC16C52



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 10-3: RESET AND DEVICE RESET TIMER - PIC16C52

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 10.1.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	100*	—	—	ns	VDD = 5 V
32	TDRT	Device Reset Timer Period	9*	18*	30*	ms	VDD = 5 V (Commercial)
34	Tioz	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low	—	—	100*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 10-5: TIMER0 CLOCK TIMINGS - PIC16C52

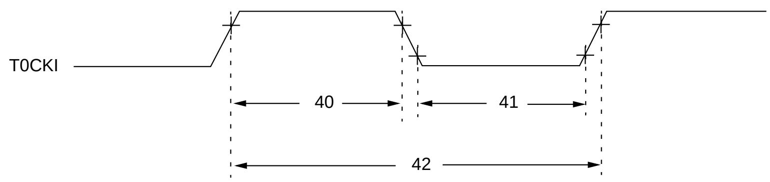


TABLE 10-4: TIMER0 CLOCK REQUIREMENTS - PIC16C52

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 10.1.					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{TCY + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

11.0 ELECTRICAL CHARACTERISTICS - PIC16C54/55/56/57

Absolute Maximum Ratings†

Ambient Temperature under bias	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on V_{DD} with respect to V_{SS}	0V to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS}(2)	0V to +14V
Voltage on all other pins with respect to V_{SS}	–0.6V to (V_{DD} + 0.6V)
Total Power Dissipation(1)	800 mW
Max. Current out of V_{SS} pin	150 mA
Max. Current into V_{DD} pin	100 mA
Max. Current into an input pin (T0CKI only)	±500 µA
Input Clamp Current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	±20 mA
Output Clamp Current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±20 mA
Max. Output Current sunk by any I/O pin	25 mA
Max. Output Current sourced by any I/O pin	20 mA
Max. Output Current sourced by a single I/O port (PORTA, B or C)	40 mA
Max. Output Current sunk by a single I/O port (PORTA, B or C)	50 mA

Note 1: Power Dissipation is calculated as follows: $Pdis = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50 to 100 Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 11-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS (RC, XT & 10) AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C5X-RC	PIC16C5X-XT	PIC16C5X-10
RC	V_{DD}: 3.0 V to 6.25 V I_{DD}: 3.3 mA max. at 5. V I_{PD}: 9 µA max. at 3.0 V, WDT dis Freq: 4 MHz max.	N/A	N/A
XT	V_{DD}: 3.0V to 6.25V I_{DD}: 1.8 mA typ. at 5.5V I_{PD}: 0.6 µA typ. at 3.0V WDT dis Freq: 4 MHz max.	V_{DD}: 3.0V to 6.25V I_{DD}: 3.3 mA max. at 5.5V I_{PD}: 9 µA max. at 3.0V, WDT dis Freq: 4 MHz max.	N/A
HS	N/A	N/A	V_{DD}: 4.5V to 5.5V I_{DD}: 10 mA max. at 5.5V I_{PD}: 9 µA max. at 3.0V, WDT dis Freq: 10 MHz max.
LP	V_{DD}: 2.5V to 6.25V I_{DD}: 15 µA typ. at 3.0V I_{PD}: 0.6 µA typ. at 3.0V, WDT dis Freq: 40 kHz max.	V_{DD}: 2.5V to 6.25V I_{DD}: 15 µA typ. at 3.0V I_{PD}: 0.6 µA typ. at 3.0V, WDT dis Freq: 40 kHz max.	V_{DD}: 2.5V to 6.25V I_{DD}: 15 µA typ. at 3.0V I_{PD}: 0.6 µA typ. at 3.0V, WDT dis Freq: 40 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

TABLE 11-2: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS (HS, LP & JW) AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C5X-HS	PIC16C5X-LP	PIC16C5X/JW
RC	N/A	N/A	V_{DD}: 3.0V to 6.25V I_{DD}: 3.3 mA max. at 5.5V I_{PD}: 9 µA max. at 3.0V, WDT dis Freq: 4 MHz max.
XT	N/A	N/A	V_{DD}: 3.0V to 6.25V I_{DD}: 3.3 mA max. at 5.5V I_{PD}: 9 µA max. at 3.0V, WDT dis Freq: 4 MHz max.
HS	V_{DD}: 4.5V to 5.5V I_{DD}: 20 mA max. at 5.5V I_{PD}: 9 µA max. at 3.0V, WDT dis Freq: 20 MHz max.	N/A	V_{DD}: 4.5V to 5.5V I_{DD}: 20 mA max. at 5.5V I_{PD}: 9 µA max. at 3.0V, WDT dis Freq: 20 MHz max.
LP	V_{DD}: 2.5V to 6.25V I_{DD}: 15 µA typ. at 3.0V I_{PD}: 0.6 µA typ. at 3.0V, WDT dis Freq: 40 kHz max.	V_{DD}: 2.5V to 6.25V I_{DD}: 32 µA max. at 32 kHz, 3.0V I_{PD}: 9 µA max. at 3.0V, WDT dis Freq: 40 kHz max.	V_{DD}: 2.5V to 6.25V I_{DD}: 32 µA max. at 32 kHz, 3.0V I_{PD}: 9 µA max. at 3.0V, WDT dis Freq: 40 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

11.1 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD		—			
PIC16C5X-RC		3.0	—	6.25	V	FOSC = DC to 4 MHz
PIC16C5X-XT		3.0	—	6.25	V	FOSC = DC to 4 MHz
PIC16C5X-10		4.5	—	5.5	V	FOSC = DC to 10 MHz
PIC16C5X-HS		4.5	—	5.5	V	FOSC = DC to 20 MHz
PIC16C5X-LP		2.5	—	6.25	V	FOSC = DC to 40 kHz
RAM Data Retention Voltage(2)	VDR		1.5*	—	V	Device in SLEEP Mode
VDD Start Voltage to ensure Power-On Reset	VPOR		VSS	—	V	See Section 7.4 for details on Power-On Reset
VDD Rise Rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-On Reset
Supply Current(3)	IDD	—				
PIC16C5X-RC(4)		—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-XT		—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-10		—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
PIC16C5X-HS		—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
		—	9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V
PIC16C5X-LP		—	15	32	μA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
Power Down Current(5)	IPD					
		—	4.0	12	μA	VDD = 3.0V, WDT enabled
		—	0.6	9	μA	VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

11.2 DC Characteristics: PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +85°C					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage PIC16C5X-RCI PIC16C5X-XTI PIC16C5X-10I PIC16C5X-HSI PIC16C5X-LPI	VDD	 3.0 3.0 4.5 4.5 2.5	 — — — — —	 6.25 6.25 5.5 5.5 6.25	 V V V V V	 FOSC = DC to 4 MHz FOSC = DC to 4 MHz FOSC = DC to 10 MHz FOSC = DC to 20 MHz FOSC = DC to 40 kHz
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD Start Voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-On Reset
VDD Rise Rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-On Reset
Supply Current(3) PIC16C5X-RCI(4) PIC16C5X-XTI PIC16C5X-10I PIC16C5X-HSI PIC16C5X-LPI	IDD	 — — — — — —	 1.8 1.8 4.8 4.8 9.0 15	 3.3 3.3 10 10 20 40	 mA mA mA mA mA µA	 FOSC = 4 MHz, VDD = 5.5V FOSC = 4 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 20 MHz, VDD = 5.5V FOSC = 32 kHz, VDD = 3.0V, WDT disabled
Power Down Current(5)	IPD	 — —	 4.0 0.6	 14 12	 µA µA	 VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

11.3 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C					
Characteristic	**Sym**	**Min**	**Typ (1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
PIC16C5X-RCE		3.25	—	6.0	V	FOSC = DC to 4 MHz
PIC16C5X-XTE		3.25	—	6.0	V	FOSC = DC to 4 MHz
PIC16C5X-10E		4.5	—	5.5	V	FOSC = DC to 10 MHz
PIC16C5X-HSE		4.5	—	5.5	V	FOSC = DC to 16 MHz
PIC16C5X-LPE		2.5	—	6.0	V	FOSC = DC to 40 kHz
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD Start Voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-On Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-On Reset
Supply Current(3)	IDD					
PIC16C5X-RCE(4)		—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-XTE		—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-10E		—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
PIC16C5X-HSE		—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
		—	9.0	20	mA	FOSC = 16 MHz, VDD = 5.5V
PIC16C5X-LPE		—	19	55	µA	FOSC = 32 kHz, VDD = 3.25V, WDT disabled
Power Down Current(5)	IPD					
		—	5.0	22	µA	VDD = 3.25V, WDT enabled
		—	0.8	18	µA	VDD = 3.25V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
   a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.
   b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

11.4 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial) PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

DC Characteristics All Pins Except Power Supply Pins	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 11.1, Section 11.2 and Section 11.3.					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		VSS	—	0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		VSS	—	0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS	—	0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS	—	0.15 VDD	V	PIC16C5X-RC only(4)
		VSS	—	0.3 VDD	V	PIC16C5X-XT, 10, HS, LP
Input High Voltage	VIH					
I/O ports		0.45 VDD	—	VDD	V	For all VDD(5)
		2.0	—	VDD	V	4.0V < VDD ≤ 5.5V(5)
		0.36 VDD	—	VDD	V	VDD > 5.5V
MCLR (Schmitt Trigger)		0.85 VDD	—	VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD	—	VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD	—	VDD	V	PIC16C5X-RC only(4)
		0.7 VDD	—	VDD	V	PIC16C5X-XT, 10, HS, LP
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*	—	—	V	
Input Leakage Current(2,3)	IIL					**For VDD ≤ 5.5V**
I/O ports		–1	0.5	+1	μA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		–5			μA	VPIN = VSS + 0.25V
			0.5	+5	μA	VPIN = VDD
T0CKI		–3	0.5	+3	μA	VSS ≤ VPIN ≤ VDD
OSC1		–3	0.5	+3	μA	VSS ≤ VPIN ≤ VDD, PIC16C5X-XT, 10, HS, LP
Output Low Voltage	VOL					
I/O ports		—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC
Output High Voltage	VOH					
I/O ports(3)		VDD – 0.7	—	—	V	IOH = –5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD – 0.7	—	—	V	IOH = –1.0 mA, VDD = 4.5V, PIC16C5X-RC

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

11.5 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Extended)

DC Characteristics All Pins Except Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C Operating Voltage VDD range is described in Section 11.1, Section 11.2 and Section 11.3.					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		Vss	—	0.15 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		Vss	—	0.15 VDD	V	
T0CKI (Schmitt Trigger)		Vss	—	0.15 VDD	V	
OSC1 (Schmitt Trigger)		Vss	—	0.15 VDD	V	PIC16C5X-RC only(4)
		Vss	—	0.3 VDD	V	PIC16C5X-XT, 10, HS, LP
Input High Voltage	VIH					
I/O ports		0.45 VDD	—	VDD	V	For all VDD(5)
		2.0	—	VDD	V	4.0V < VDD ≤ 5.5V(5)
		0.36 VDD	—	VDD	V	VDD > 5.5 V
MCLR (Schmitt Trigger)		0.85 VDD	—	VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD	—	VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD	—	VDD	V	PIC16C5X-RC only(4)
		0.7 VDD	—	VDD	V	PIC16C5X-XT, 10, HS, LP
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*	—	—	V	
Input Leakage Current (2,3)	IIL					**For VDD ≤ 5.5 V**
I/O ports		–1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		–5			µA	VPIN = VSS + 0.25V
			0.5	+5	µA	VPIN = VDD
T0CKI		–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
OSC1		–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD, PIC16C5X-XT, 10, HS, LP
Output Low Voltage	VOL					
I/O ports		—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC
Output High Voltage	VOH					
I/O ports(3)		VDD – 0.7	—	—	V	IOH = –5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD – 0.7	—	—	V	IOH = –1.0 mA, VDD = 4.5V, PIC16C5X-RC

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

11.6 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

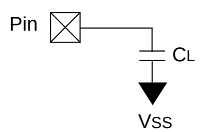
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 11-1: LOAD CONDITIONS - PIC16C54/55/56/57



C_L = 50 pF for all pins except OSC2

15 pF for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1

11.7 Timing Diagrams and Specifications

FIGURE 11-2: EXTERNAL CLOCK TIMING - PIC16C54/55/56/57

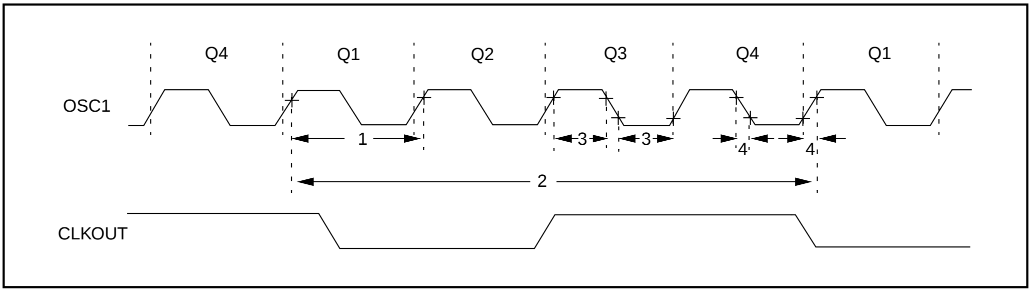


TABLE 11-3: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 11.1, Section 11.2 and Section 11.3

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
	FOSC	External CLKIN Frequency(2)	DC	—	4	MHz	XT osc mode
			DC	—	10	MHz	10 MHz mode
			DC	—	20	MHz	HS osc mode (Com/Indust)
			DC	—	16	MHz	HS osc mode (Extended)
			DC	—	40	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	10	MHz	10 MHz mode
			4	—	20	MHz	HS osc mode (Com/Indust)
			4	—	16	MHz	HS osc mode (Extended)
			DC	—	40	kHz	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

TABLE 11-3: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57 (CON'T)

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 11.1, Section 11.2 and Section 11.3						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
1	TOSC	External CLKIN Period(2)	250	—	—	ns	XT osc mode
			100	—	—	ns	10 MHz mode
			50	—	—	ns	HS osc mode (Com/Indust)
			62.5	—	—	ns	HS osc mode (Extended)
			25	—	—	μs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			100	—	250	ns	10 MHz mode
			50	—	250	ns	HS osc mode (Com/Indust)
			62.5	—	250	ns	HS osc mode (Extended)
			25	—	—	μs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2*	—	—	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

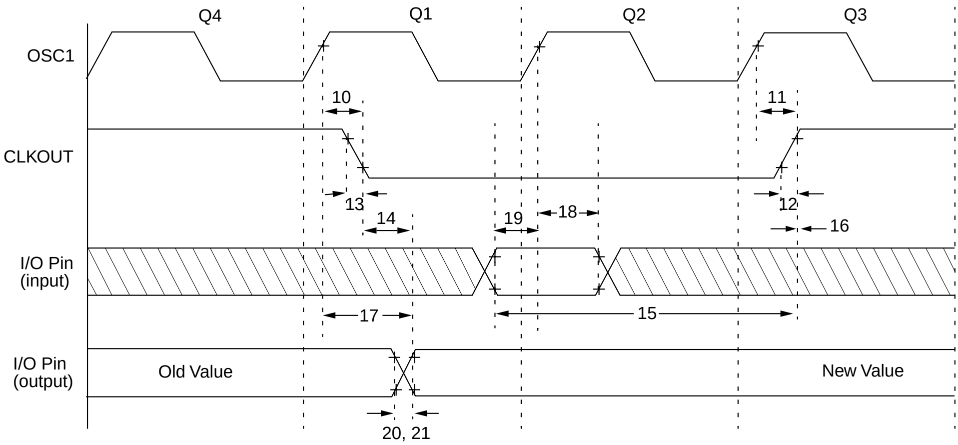
* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 11-3: CLKOUT AND I/O TIMING - PIC16C54/55/56/57



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

TABLE 11-4: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54/55/56/57

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 11.1, Section 11.2 and Section 11.3					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5	15**	ns
13	TckF	CLKOUT fall time(2)	—	5	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

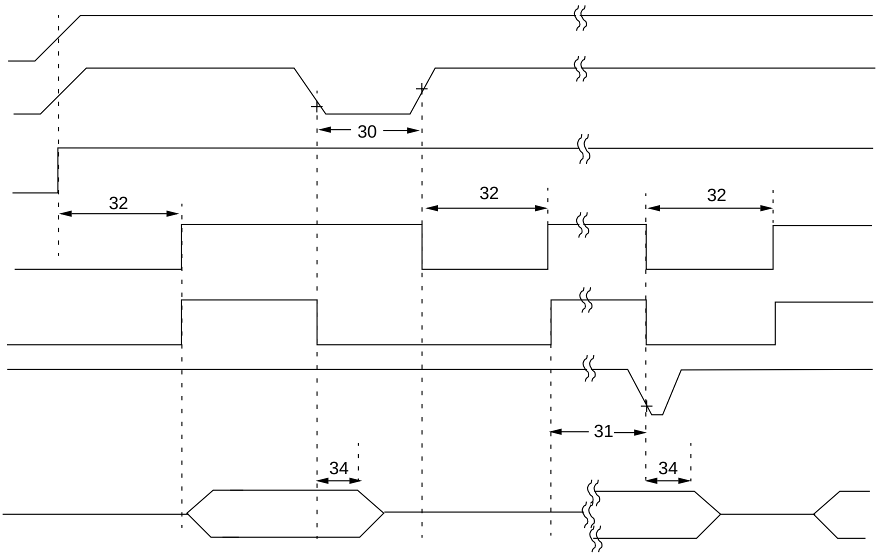
** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 11-1 for loading conditions.

FIGURE 11-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54/55/56/57



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 11-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54/55/56/57

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 11.1, Section 11.2 and Section 11.3						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TmcL	MCLR Pulse Width (low)	100*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9*	18*	30*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	9*	18*	30*	ms	VDD = 5.0V (Commercial)
34	Tioz	I/O Hi-impedance from MCLR Low	—	—	100*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 11-5: TIMER0 CLOCK TIMINGS - PIC16C54/55/56/57

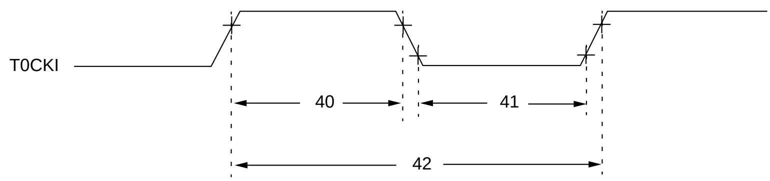


TABLE 11-6: TIMER0 CLOCK REQUIREMENTS - PIC16C54/55/56/57

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 11.1, Section 11.2 and Section 11.3						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or (TCY + 40)/N*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NOTES:

12.0 DC AND AC CHARACTERISTICS - PIC16C54/55/56/57

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean – 3σ) respectively, where σ is standard deviation.

FIGURE 12-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

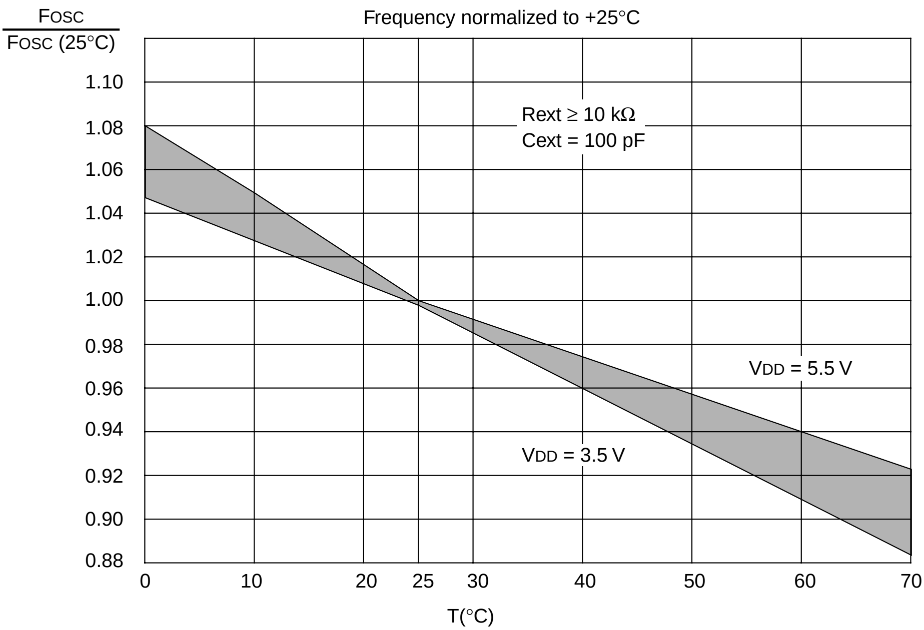


TABLE 12-1: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5 V, 25°C	
20 pF	3.3 k	4.973 MHz	± 27%
	5 k	3.82 MHz	± 21%
	10 k	2.22 MHz	± 21%
	100 k	262.15 kHz	± 31%
100 pF	3.3 k	1.63 MHz	± 13%
	5 k	1.19 MHz	± 13%
	10 k	684.64 kHz	± 18%
	100 k	71.56 kHz	± 25%
300 pF	3.3 k	660 kHz	± 10%
	5.0 k	484.1 kHz	± 14%
	10 k	267.63 kHz	± 15%
	160 k	29.44 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5 V.

FIGURE 12-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF

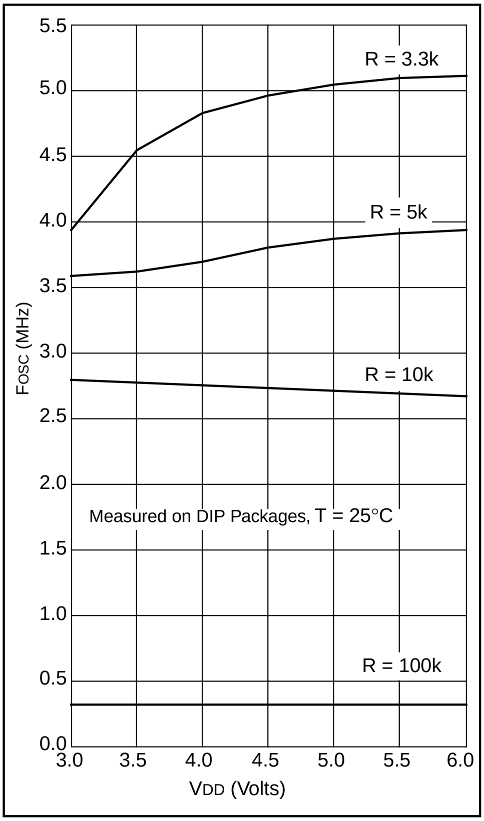


FIGURE 12-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF

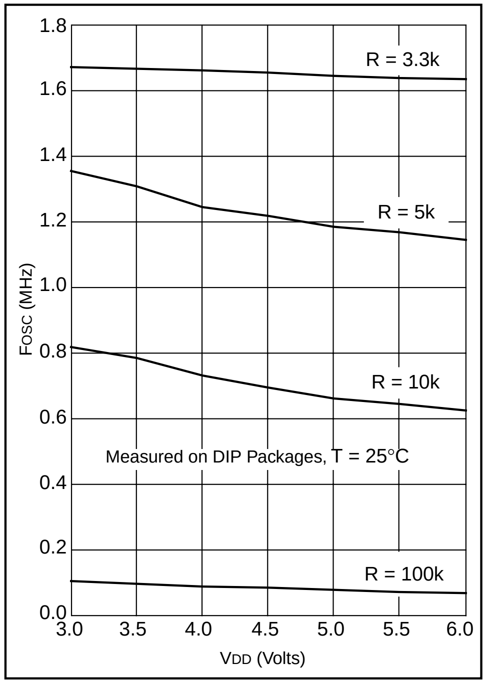
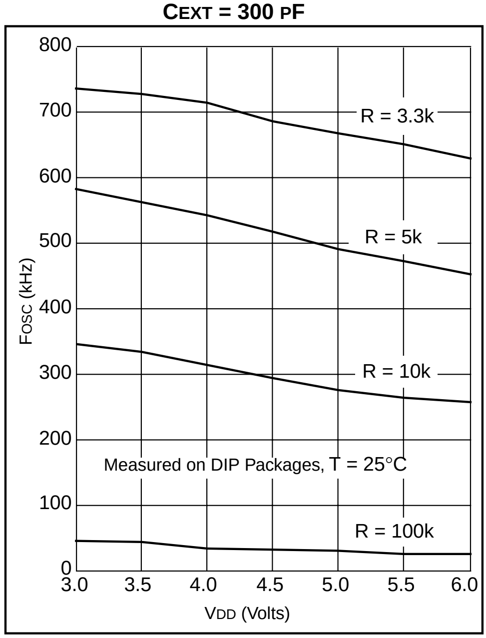


FIGURE 12-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF



Preliminary

FIGURE 12-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED

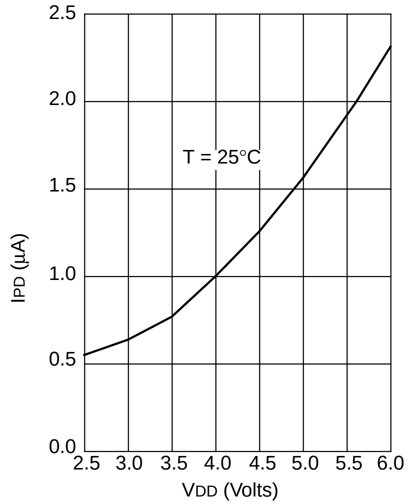


FIGURE 12-7: TYPICAL IPD vs. VDD, WATCHDOG ENABLED

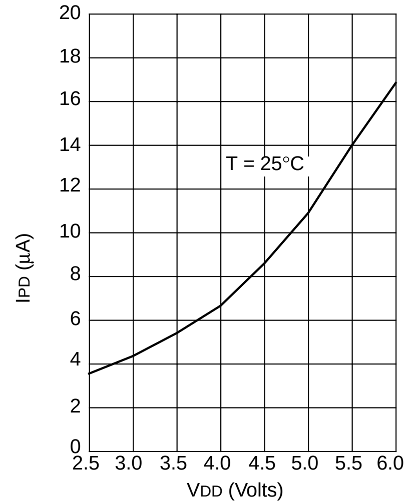


FIGURE 12-6: MAXIMUM IPD vs. VDD, WATCHDOG DISABLED

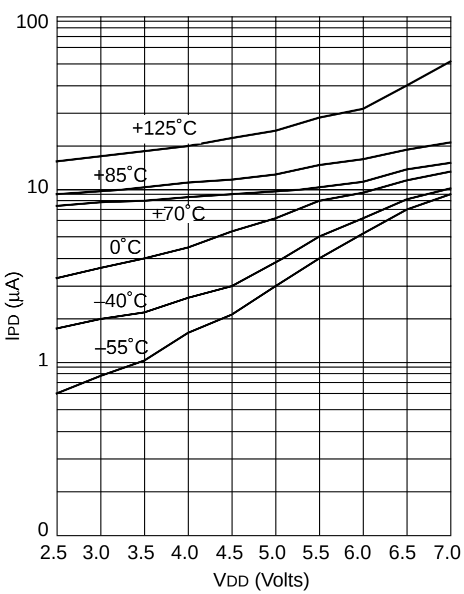
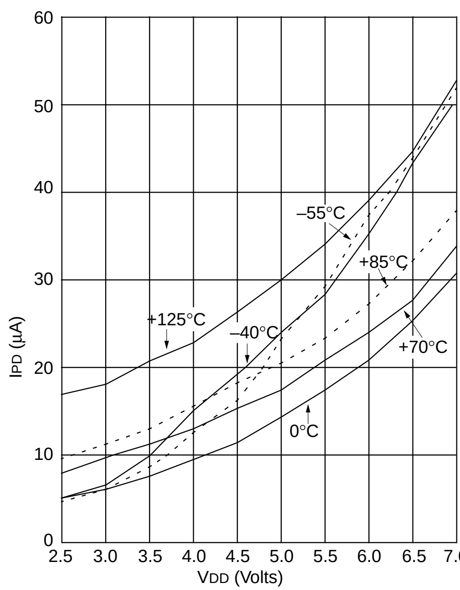


FIGURE 12-8: MAXIMUM IPD vs. VDD, WATCHDOG ENABLED



IPD, with WDT enabled, has two components:

The leakage current which increases with higher temperature and the operating current of the WDT logic which increases with lower temperature. At –40°C, the latter dominates explaining the apparently anomalous behavior.

FIGURE 12-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs. VDD

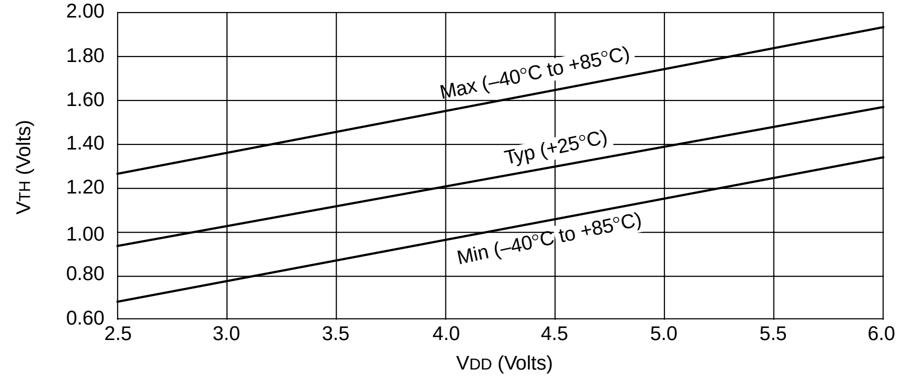
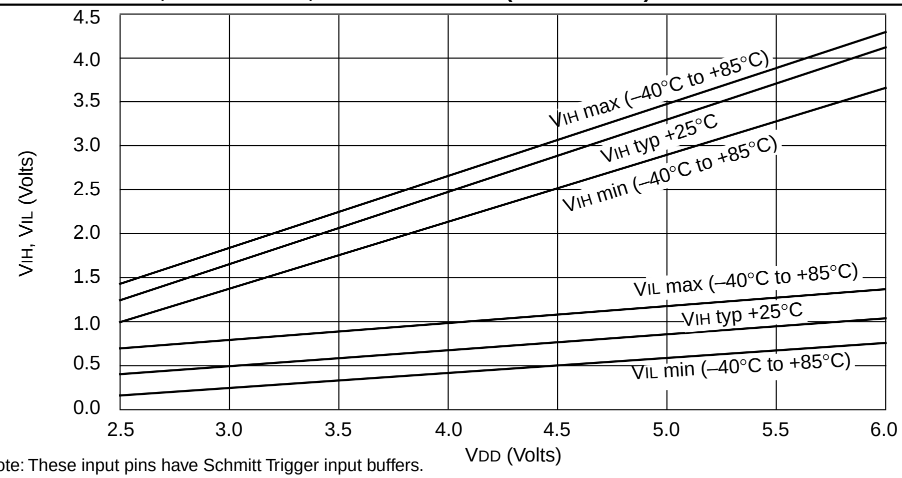


FIGURE 12-10: VIH, VIL OF $\overline{\text{MCLR}}$, T0CKI AND OSC1 (IN RC MODE) vs. VDD



Note: These input pins have Schmitt Trigger input buffers.

FIGURE 12-11: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs. VDD

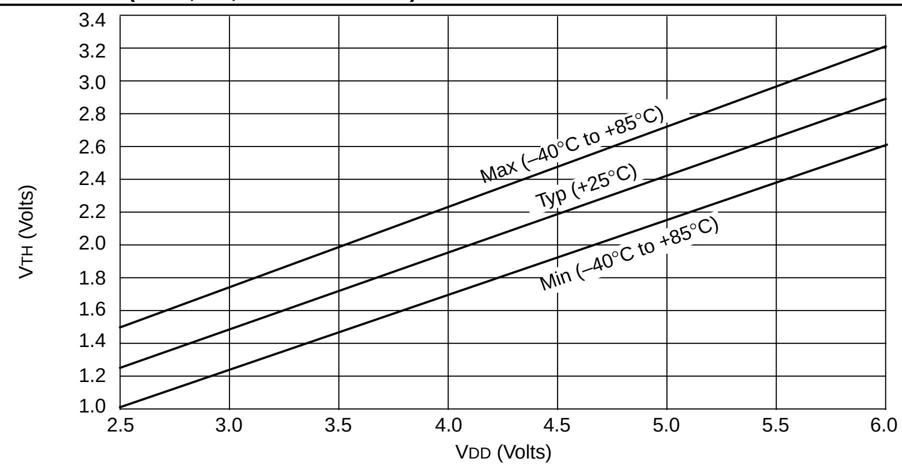


FIGURE 12-12: TYPICAL IDD vs. FREQUENCY (EXTERNAL CLOCK, 25°C)

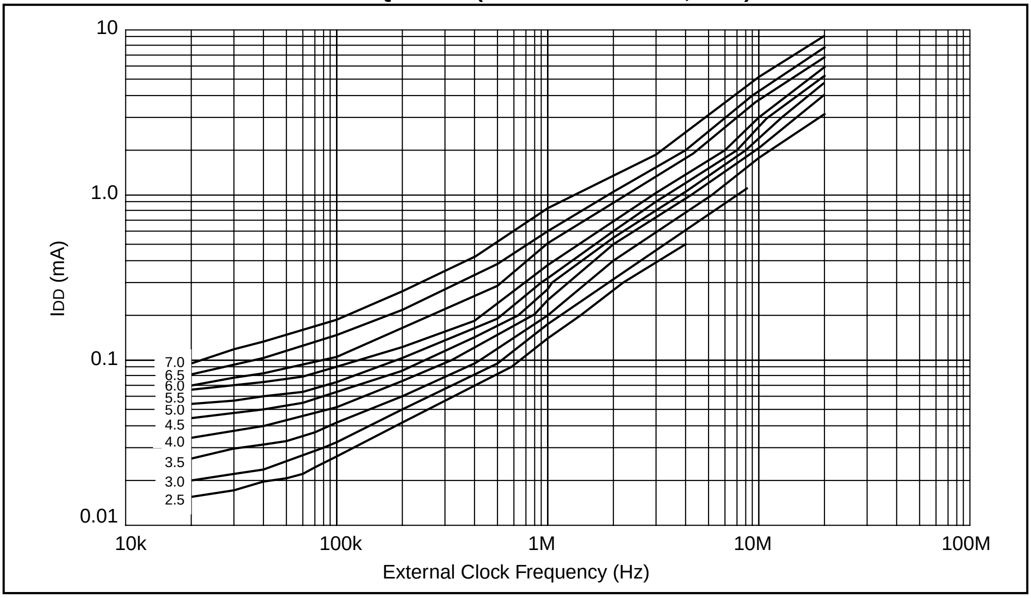


FIGURE 12-13: MAXIMUM IDD vs. FREQUENCY (EXTERNAL CLOCK, –40°C TO +85°C)

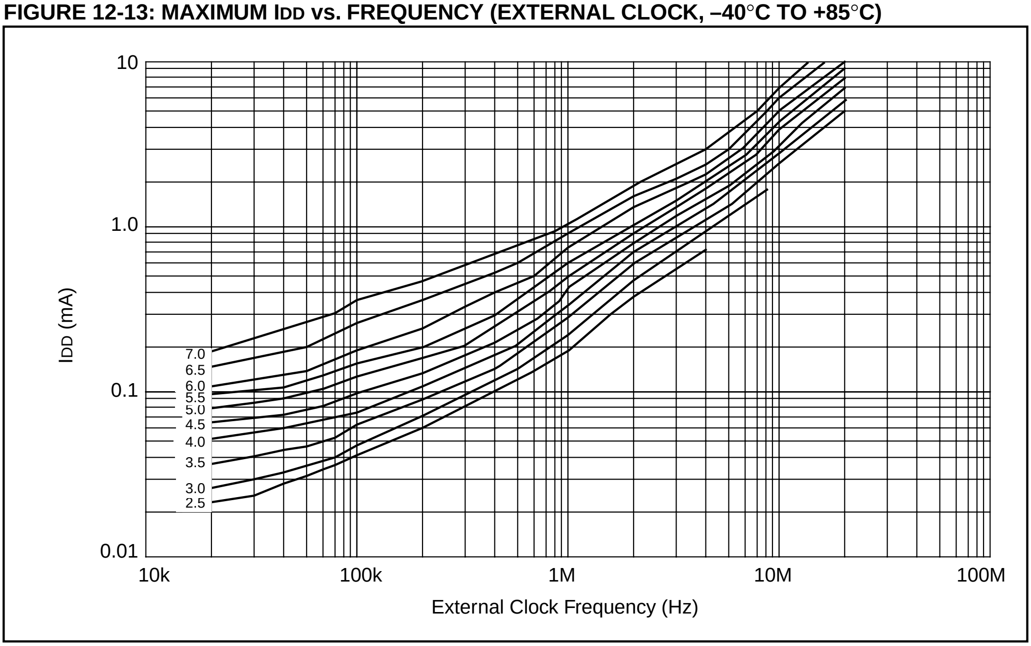


FIGURE 12-14: MAXIMUM IDD vs. FREQUENCY (EXTERNAL CLOCK –55°C TO +125°C)

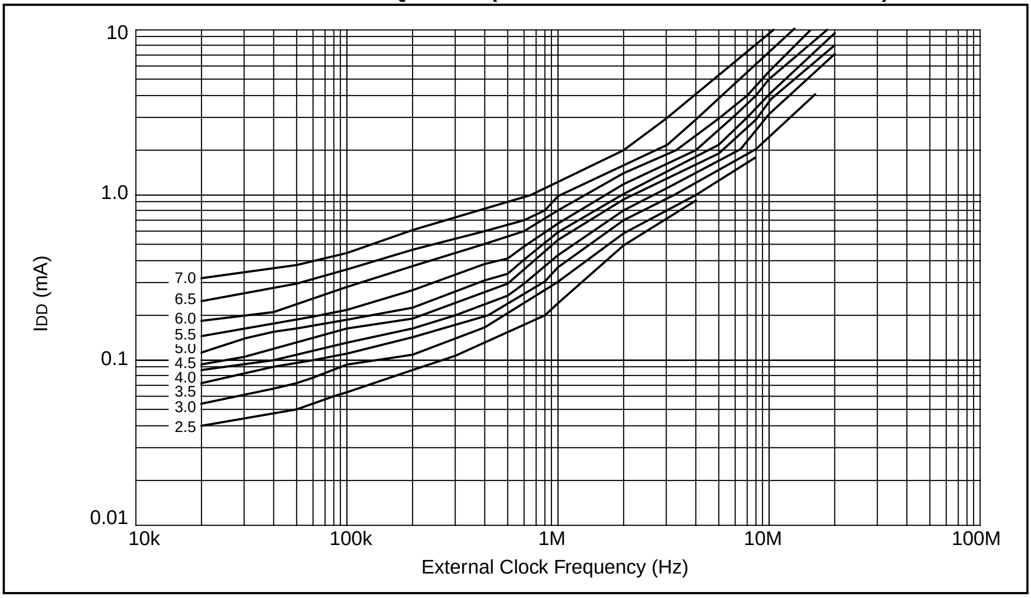


FIGURE 12-15: WDT TIMER TIME-OUT PERIOD vs. VDD

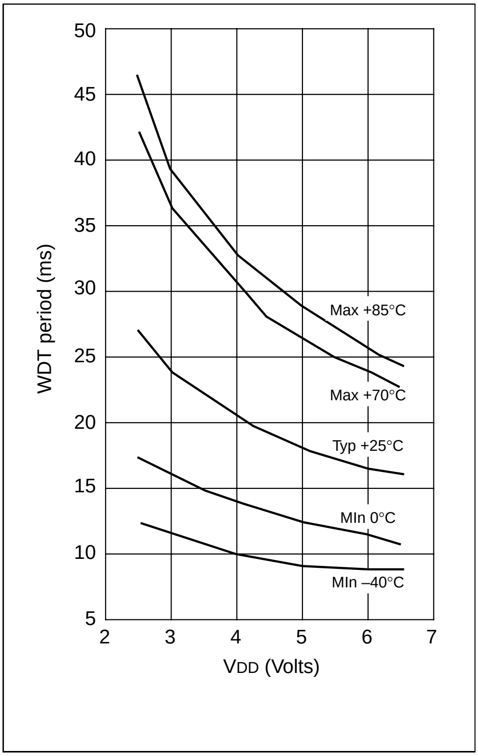
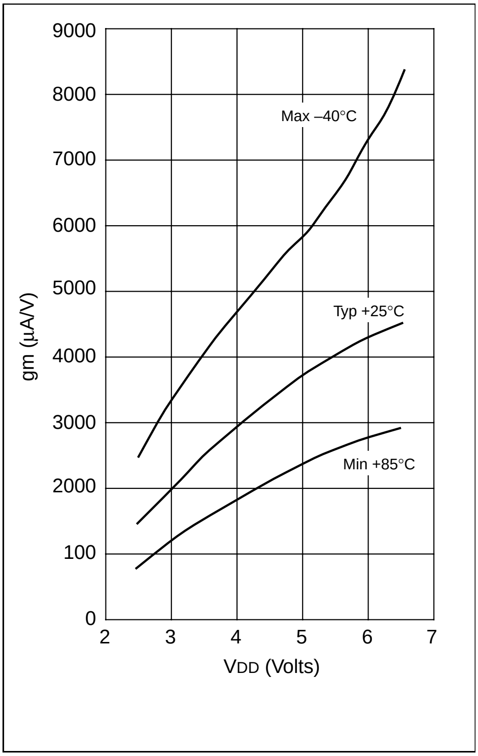


FIGURE 12-16: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD



 Preliminary

FIGURE 12-17: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

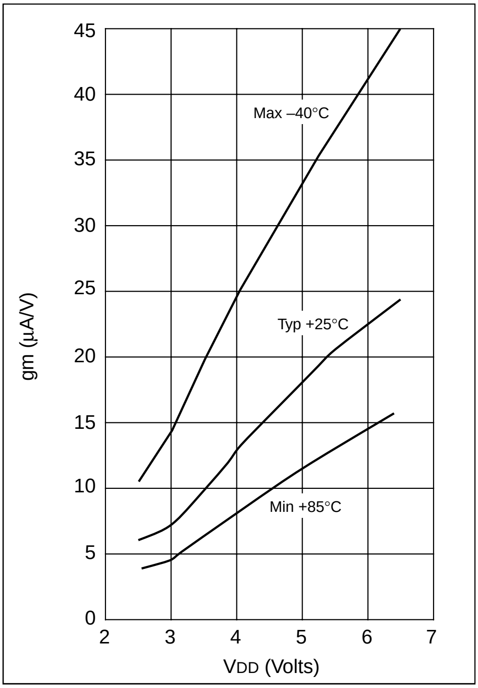


FIGURE 12-18: IOH vs. VOH, VDD = 3 V

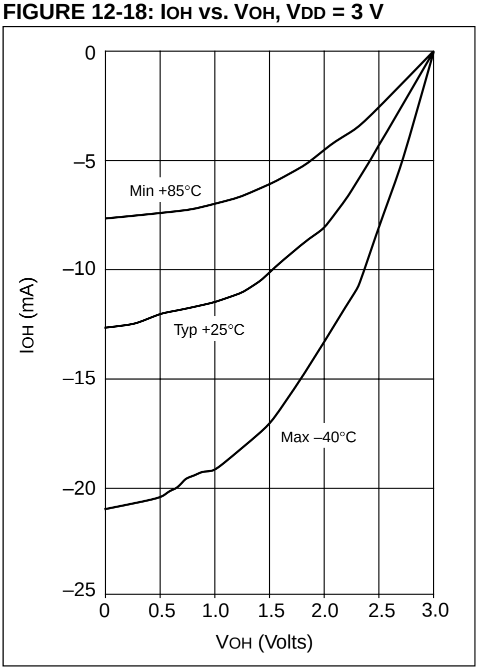


FIGURE 12-19: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD

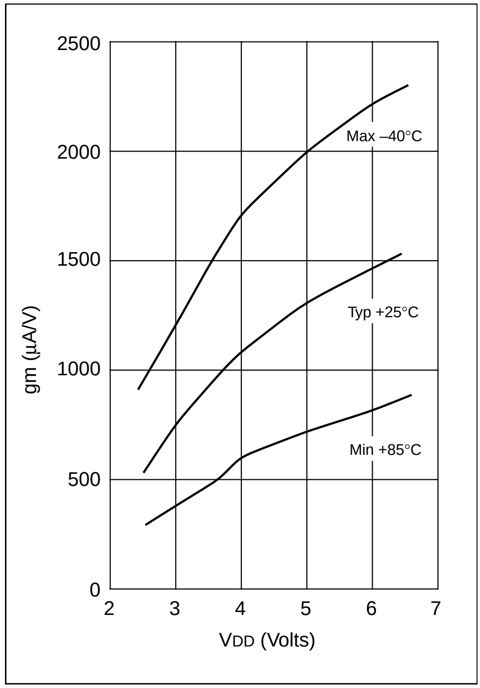


FIGURE 12-20: IOH vs. VOH, VDD = 5 V

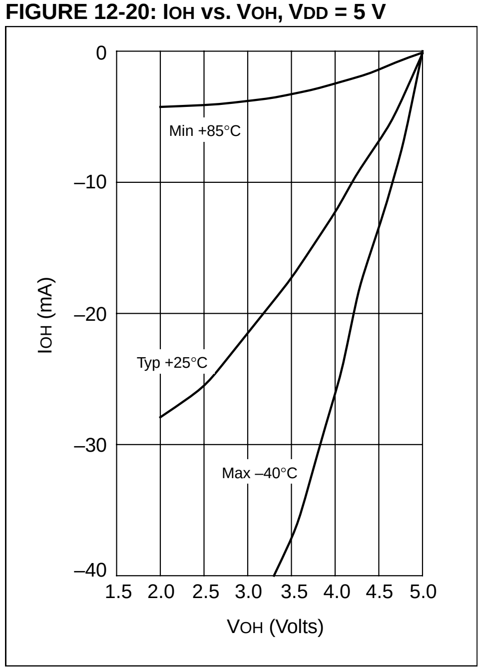


FIGURE 12-21: IOL vs. VOL, VDD = 3 V

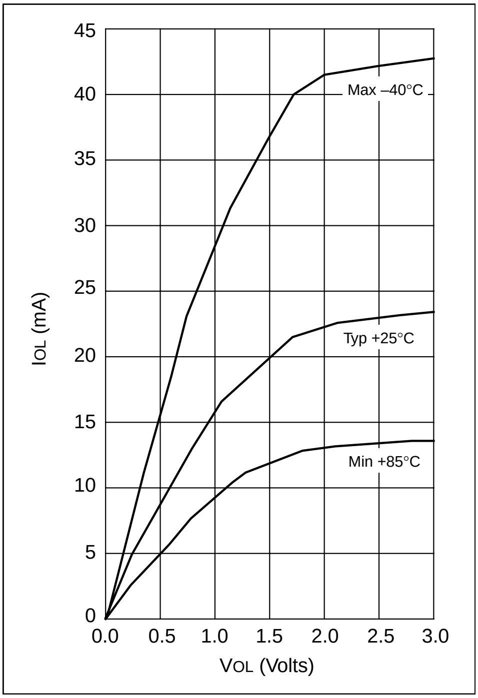


FIGURE 12-22: IOL vs. VOL, VDD = 5 V

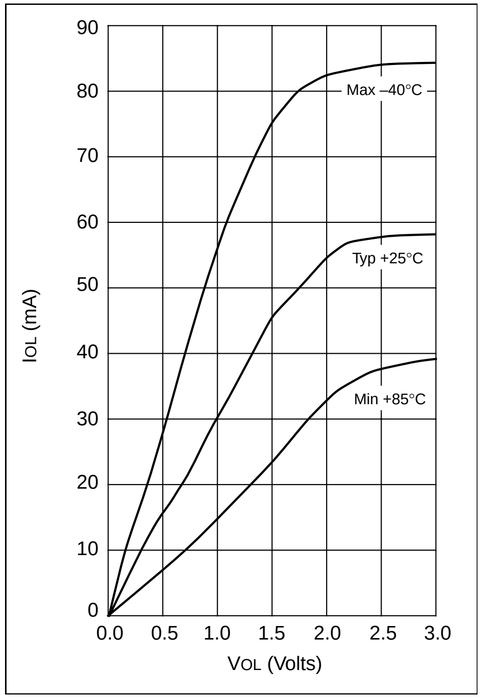


TABLE 12-2: INPUT CAPACITANCE FOR PIC16C54/56

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{\text{MCLR}}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

TABLE 12-3: INPUT CAPACITANCE FOR PIC16C55/57

Pin	Typical Capacitance (pF)	
	28L PDIP (600 mil)	28L SOIC
RA port	5.2	4.8
RB port	5.6	4.7
RC port	5.0	4.1
$\overline{\text{MCLR}}$	17.0	17.0
OSC1	6.6	3.5
OSC2/CLKOUT	4.6	3.5
T0CKI	4.5	3.5

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

13.0 ELECTRICAL CHARACTERISTICS - PIC16CR54A

Absolute Maximum Ratings†

Ambient Temperature under bias .... –55°C to +125°C
Storage Temperature .... –65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} .... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS}(2) .... 0 to +14V
Voltage on all other pins with respect to V_{SS} .... –0.6V to (V_{DD} + 0.6V)
Total Power Dissipation(1) .... 800 mW
Max. Current out of V_{SS} pin .... 150 mA
Max. Current into V_{DD} pin .... 50 mA
Max. Current into an input pin (T0CKI only) .... ±500 μA
Input Clamp Current, I_{IK} (V_I < 0 or V_I > V_{DD}) .... ±20 mA
Output Clamp Current, I_{OK} (V0 < 0 or V0 > V_{DD}) .... ±20 mA
Max. Output Current sunk by any I/O pin .... 25 mA
Max. Output Current sourced by any I/O pin .... 20 mA
Max. Output Current sourced by a single I/O port (PORTA or B) .... 40 mA
Max. Output Current sunk by a single I/O port (PORTA or B) .... 50 mA

Note 1: Power Dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below Vss at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50 to 100Ω should be used when applying a low level to the $\overline{MCLR}$ pin rather than pulling this pin directly to Vss.

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 13-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16CR54A-04	PIC16CR54A-10	PIC16CR54A-20	PIC16LCR54A-04
RC	V_{DD}: 2.5 V to 6.25 V I_{DD}: 3.6 mA max at 6.0 V I_{PD}: 6.0 μA max at 2.5 V, WDT dis Freq: 4 MHz max	N/A	N/A	N/A
XT	V_{DD}: 2.5 V to 6.25 V I_{DD}: 3.6 mA max at 6.0 V I_{PD}: 6.0 μA max at 2.5 V, WDT dis Freq: 4.0 MHz max	N/A	N/A	N/A
HS	N/A	V_{DD}: 4.5 V to 5.5 V I_{DD}: 10 mA max at 5.5 V I_{PD}: 6.0 μA max at 2.5 V, WDT dis Freq: 10 MHz max	V_{DD}: 4.5 V to 5.5 V I_{DD}: 10 mA max at 5.5 V I_{PD}: 6.0 μA max at 2.5 V, WDT dis Freq: 20 MHz max	N/A
LP	N/A	N/A	N/A	V_{DD}: 2.0 V to 6.25 V I_{DD}: 20 μA max at 32 kHz, 2.0 V I_{PD}: 6.0 μA max at 2.5 V, WDT dis Freq: 200 kHz max

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

Preliminary

13.1 DC Characteristics: PIC16CR54A-04, 10, 20 (Commercial) PIC16CR54A-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage RC and XT options HS option	VDD	 2.5 4.5		 6.25 5.5	 V V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) RC(4) and XT options HS option	IDD		 2.0 0.8 90 4.8 9.0	 3.6 1.8 350 10 20	 mA mA µA mA mA	 FOSC = 4.0 MHz, VDD = 6.0V FOSC = 4.0 MHz, VDD = 3.0V FOSC = 200 kHz, VDD = 2.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 20 MHz, VDD = 5.5V
Power-Down Current(5) Commercial	IPD		 1.0 2.0 3.0 5.0	 6.0 8.0* 15 25	 µA µA µA µA	 VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled
Power-Down Current(5) Industrial	IPD		 1.0 2.0 3.0 3.0 5.0	 8.0 10* 20* 18 45	 µA µA µA µA µA	 VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 4.0V, WDT enabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

13.2 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (extended)			
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
RC, XT and LP options		3.25	—	6.0	V	
HS options		4.5	—	5.5	V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
RC(4) and XT options		—	1.8	3.3	mA	FOSC = 4.0 MHz, VDD = 5.5V
HS option		—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
		—	9.0	20	mA	FOSC = 16 MHz, VDD = 5.5V
Power-Down Current(5)	IPD					
		—	5.0	22	μA	VDD = 3.25V, WDT enabled
		—	0.8	18	μA	VDD = 3.25V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

13.3 DC Characteristics: PIC16LCR54A-04 (Commercial) PIC16LCR54A-04I (Industrial)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	2.0	—	6.25	V	LP Option
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD	—	 10	 20 70	 µA µA	 FOSC = 32 kHz, VDD = 2.0V FOSC = 32 kHz, VDD = 6.0V
Power-Down Current(5) Commercial	IPD	 — — — —	 1.0 2.0 3.0 5.0	 6.0 8.0* 15 25	 µA µA µA µA	 VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled
Power-Down Current(5) Industrial	IPD	 — — — — —	 1.0 2.0 3.0 3.0 5.0	 8.0 10* 20* 18 45	 µA µA µA µA µA	 VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 4.0V, WDT enabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

13.4 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

DC Characteristics All Pins Except Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 13.1 and Section 13.3.					
Characteristic	**Sym**	**Min**	**Typ[(1)]**	**Max**	**Units**	**Conditions**
Input Low Voltage	V_{IL}					
I/O ports		V_{SS}	—	0.2 V_{DD}	V	Pin at hi-impedance
$\overline{MCLR}$ (Schmitt Trigger)		V_{SS}	—	0.15 V_{DD}	V	
T0CKI (Schmitt Trigger)		V_{SS}	—	0.15 V_{DD}	V	
OSC1 (Schmitt Trigger)		V_{SS}	—	0.15 V_{DD}	V	RC option only[(4)]
OSC1		V_{SS}	—	0.15 V_{DD}	V	XT, HS and LP options
Input High Voltage	V_{IH}					
I/O ports		2.0	—	V_{DD}	V	V_{DD} = 3.0V to 5.5V[(5)]
		0.6 V_{DD}	—	V_{DD}	V	Full V_{DD} range[(5)]
$\overline{MCLR}$ (Schmitt Trigger)		0.85 V_{DD}	—	V_{DD}	V	
T0CKI (Schmitt Trigger)		0.85 V_{DD}	—	V_{DD}	V	
OSC1 (Schmitt Trigger)		0.85 V_{DD}	—	V_{DD}	V	RC option only[(4)]
OSC1		0.85 V_{DD}	—	V_{DD}	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	V_{HYS}	0.15V_{DD}*	—	—	V	
Input Leakage Current[(3)]	I_{IL}					**For V_{DD} ≤ 5.5V**
I/O ports		–1.0		+1.0	μA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at hi-impedance
$\overline{MCLR}$		–5.0			μA	$V_{PIN} = V_{SS}$ + 0.25V[(2)]
			0.5	+5.0	μA	$V_{PIN} = V_{DD}$[(2)]
T0CKI		–3.0	0.5	+3.0	μA	$V_{SS} \le V_{PIN} \le V_{DD}$
OSC1		–3.0	0.5	+3.0	μA	$V_{SS} \le V_{PIN} \le V_{DD}$, XT, HS and LP options
Output Low Voltage	V_{OL}					
I/O ports		—	—	0.5	V	I_{OL} = 10 mA, V_{DD} = 6.0V
OSC2/CLKOUT		—	—	0.5	V	I_{OL} = 1.9 mA, V_{DD} = 6.0V, RC option only
Output High Voltage[(3)]	V_{OH}					
I/O ports		V_{DD} –0.5	—	—	V	I_{OH} = –4.0 mA, V_{DD} = 6.0V
OSC2/CLKOUT		V_{DD} –0.5	—	—	V	I_{OH} = –0.8 mA, V_{DD} = 6.0V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

13.5 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

DC Characteristics All Pins Except Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C Operating Voltage VDD range is described in Section 13.2.					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		Vss	—	0.15 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		Vss	—	0.15 VDD	V	
T0CKI (Schmitt Trigger)		Vss	—	0.15 VDD	V	
OSC1 (Schmitt Trigger)		Vss	—	0.15 VDD	V	RC option only(4)
OSC1		Vss	—	0.3 VDD	V	XT, HS and LP options
Input High Voltage	VIH					
I/O ports		0.45 VDD	—	VDD	V	For all VDD(5)
		2.0	—	VDD	V	4.0V < VDD ≤ 5.5V(5)
		0.36 VDD	—	VDD	V	VDD > 5.5V
MCLR (Schmitt Trigger)		0.85 VDD	—	VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD	—	VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD	—	VDD	V	RC option only(4)
OSC1		0.7 VDD	—	VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*	—	—	V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		–1.0	0.5	+1.0	μA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		–5.0			μA	VPIN = VSS + 0.25V(2)
			0.5	+5.0	μA	VPIN = VDD(2)
T0CKI		–3.0	0.5	+3.0	μA	VSS ≤ VPIN ≤ VDD
OSC1		–3.0	0.5	+3.0	μA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports		—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage (3)	VOH					
I/O ports		VDD –0.7	—	—	V	IOH = –5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD –0.7	—	—	V	IOH = –1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

13.6 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

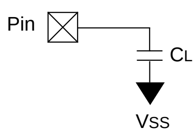
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 13-1: LOAD CONDITIONS



C_L = 50 pF for all pins except OSC2
15 pF for OSC2 in XT, HS or LP options when external clock is used to drive OSC1

13.7 Timing Diagrams and Specifications

FIGURE 13-2: EXTERNAL CLOCK TIMING - PIC16CR54A

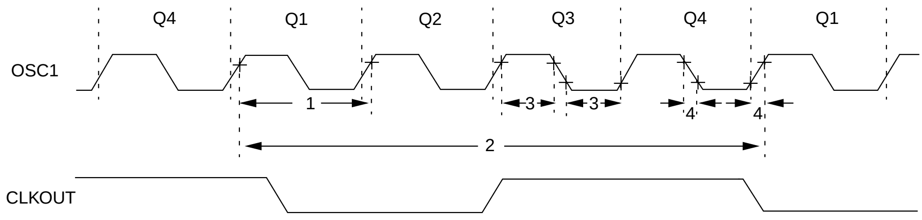


TABLE 13-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A

AC Characteristics — **Standard Operating Conditions (unless otherwise specified)**
Operating Temperature 0°C ≤ TA ≤ +70°C (commercial)
–40°C ≤ TA ≤ +85°C (industrial)
–40°C ≤ TA ≤ +125°C (extended)
Operating Voltage VDD range is described in Section 13.1, Section 13.2 and Section 13.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
	FOSC	External CLKIN Frequency(2)	DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	10	MHz	HS osc mode (10)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4.0	MHz	RC osc mode
			0.1	—	4.0	MHz	XT osc mode
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	10	MHz	HS osc mode (10)
			4.0	—	20	MHz	HS osc mode (20)
			5.0	—	200	kHz	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

TABLE 13-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A (CON'T)

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 13.1, Section 13.2 and Section 13.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
1	TOSC	External CLKIN Period(2)	250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			100	—	—	ns	HS osc mode (10)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	μs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			100	—	250	ns	HS osc mode (10)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	μs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

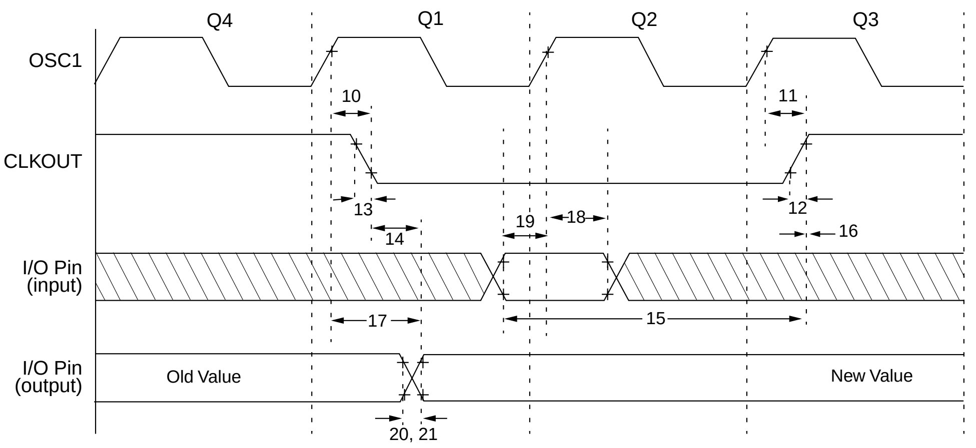
* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 13-3: CLKOUT AND I/O TIMING - PIC16CR54A



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

TABLE 13-3: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR54A

AC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 13.1, Section 13.2 and Section 13.3.				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time(2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

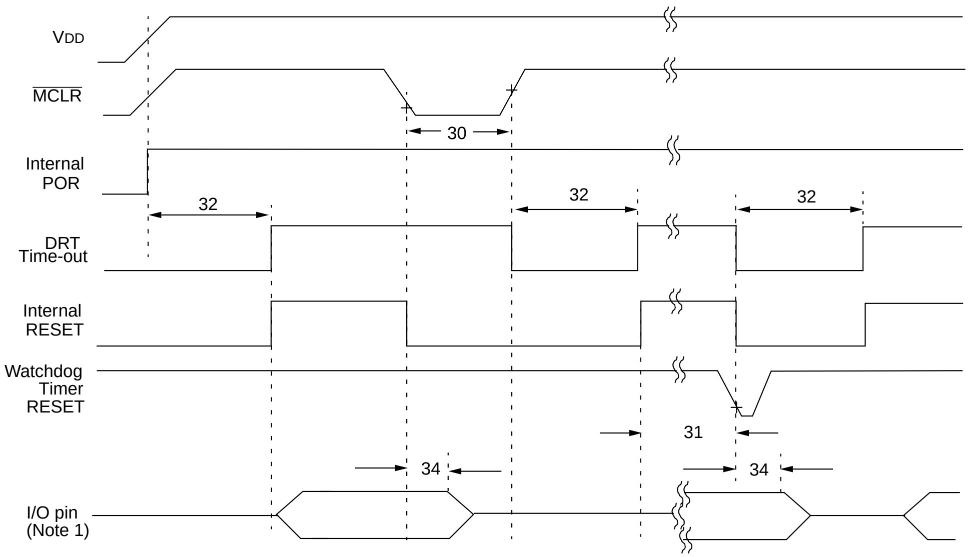
** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 13-1 for loading conditions.

FIGURE 13-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR54A



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 13-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR54A

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 13.1, Section 13.2 and Section 13.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	1.0*	—	—	µs	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7.0*	18*	40*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	7.0*	18*	30*	ms	VDD = 5.0V (Commercial)
34	TioZ	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low	—	—	1.0*	µs	

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Preliminary

FIGURE 13-5: TIMER0 CLOCK TIMINGS - PIC16CR54A

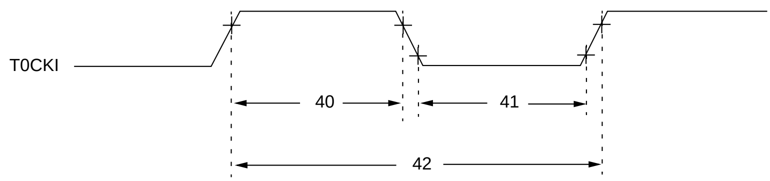


TABLE 13-5: TIMER0 CLOCK REQUIREMENTS - PIC16CR54A

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 13.1, Section 13.2 and Section 13.3.					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{TCY + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NOTES:

14.0 ELECTRICAL CHARACTERISTICS - PIC16C54A

Absolute Maximum Ratings†

Ambient temperature under bias .... –55°C to +125°C
Storage temperature .... –65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} .... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} .... 0 to +14V
Voltage on all other pins with respect to V_{SS} .... –0.6V to (V_{DD} + 0.6V)
Total power dissipation(1) .... 800 mW
Max. current out of V_{SS} pin .... 150 mA
Max. current into V_{DD} pin .... 100 mA
Max. current into an input pin (T0CKI only) .... ±500 µA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) .... ±20 mA
Max. output current sunk by any I/O pin .... 25 mA
Max. output current sourced by any I/O pin .... 20 mA
Max. output current sourced by a single I/O port (PORTA or B) .... 50 mA
Max. output current sunk by a single I/O port (PORTA or B) .... 50 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 14-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C54A-04	PIC16C54A-10	PIC16C54A-20	PIC16LC54A-04
RC	VDD: 3.0V to 6.25V IDD: 2.4 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 4 MHz max.	VDD: 3.0V to 6.25V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 0.5 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.
XT	VDD: 3.0V to 6.25V IDD 2.4 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 4 MHz max.	VDD: 3.0V to 6.25V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 0.5 mA typ. at 5.5V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 4.0 MHz max.
HS	N/A	VDD: 4.5V to 5.5V IDD: 8.0 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 16 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 20 MHz max.	Do not use in HS mode
LP	VDD: 3.0V to 6.25V IDD: 14 µA typ. at 32kHz, 3.0V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 200 kHz max.	Do not use in LP mode	Do not use in LP mode	VDD: 2.5V to 6.25V IDD: 27 µA max. at 32kHz, 2.5V WDT dis IPD: 4.0 µA max. at 2.5V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

OSC	PIC16C54A/JW	PIC16LV54A-02
RC	VDD: 3.0V to 6.25V IDD: 2.4 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 2.0V to 3.8V IDD: 0.5 mA typ. at 3.0V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 2.0 MHz max.
XT	VDD: 3.0V to 6.25V IDD 2.4 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 2.0V to 3.8V IDD: 0.5 mA typ. at 3.0V IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 2.0 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 8 mA max. at 5.5V IPD: 4.0 µA max. at 3.0V WDT dis Freq: 10 MHz max.	Do not use in HS mode
LP	VDD: 2.5V to 6.25V IDD: 27 µA max. at 32kHz, 2.5V WDT dis IPD: 4.0 µA max. at 2.5V WDT dis Freq: 200 kHz max.	VDD: 2.0V to 3.8V IDD: 27 µA max. at 32kHz, 2.5V WDT dis IPD: 4.0 µA max. at 2.5V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

14.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
XT, RC and LP options		3.0	—	6.25	V	
HS option		4.5	—	5.5	V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
XT and RC(4) options		—	1.8	2.4	mA	FOSC = 4.0 MHz, VDD = 5.5V
HS option		—	2.4	8.0	mA	FOSC = 10 MHz, VDD = 5.5V
		—	4.5	16	mA	FOSC = 20 MHz, VDD = 5.5V
LP option, Commercial		—	14	29	μA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
LP option, Industrial		—	17	37	μA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
Power Down Current(5)	IPD					
Commercial		—	4.0	12	μA	VDD = 3.0V, WDT enabled
		—	0.25	4.0	μA	VDD = 3.0V, WDT disabled
Industrial		—	5.0	14	μA	VDD = 3.0V, WDT enabled
		—	0.3	5.0	μA	VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

14.2 DC Characteristics: PIC16C54A-04E, 10E, 20E (Extended)

DC Characteristics Power Supply Pins						Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended)
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage XT and RC options HS option	V_{DD}	 3.5 4.5	 — —	 5.5 5.5	 V V	
RAM Data Retention Voltage(2)	V_{DR}	—	1.5*	—	V	Device in SLEEP mode
V_{DD} start voltage to ensure Power-On Reset	V_{POR}	—	V_{SS}	—	V	See Section 7.4 for details on Power-on Reset
V_{DD} rise rate to ensure Power-On Reset	S_{VDD}	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) XT and RC(4) options HS option 	I_{DD}	 — — —	 1.8 4.8 9.0	 3.3 10 20	 mA mA mA	 F_{OSC} = 4.0 MHz, V_{DD} = 5.5V F_{OSC} = 10 MHz, V_{DD} = 5.5V F_{OSC} = 20 MHz, V_{DD} = 5.5V
Power Down Current(5) XT and RC options HS option 	I_{PD}	 — — — —	 5.0 0.8 4.0 0.25	 22 18 22 18	 μA μA μA μA	 V_{DD} = 3.5V, WDT enabled V_{DD} = 3.5V, WDT disabled V_{DD} = 3.5V, WDT enabled V_{DD} = 3.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{SS}, T0CKI = V_{DD}, $\overline{MCLR}$ = V_{DD}; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2Rext$ (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} and V_{SS}.

14.3 DC Characteristics: PIC16LC54A-04 (Commercial)
PIC16LC54A-04I (Industrial)
PIC16LC54A-04E (Extended)

DC Characteristics **Power Supply Pins**	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended)					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage XT, RC and LP options	VDD	 2.5	 —	 6.25	 V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) XT and RC(4) options LP option, Commercial LP option, Industrial LP option, Extended	IDD	 — — — —	 0.5 11 11 11	 25 27 35 37	 mA µA µA µA	 FOSC = 4.0 MHz, VDD = 5.5V FOSC = 32 kHz, VDD = 2.5V WDT disabled FOSC = 32 kHz, VDD = 2.5V WDT disabled FOSC = 32 kHz, VDD = 2.5V WDT disabled
Power Down Current(5) Commercial Industrial Extended 	IPD	 — — — — — —	 2.5 0.25 2.5 0.25 2.5 0.25	 12 4.0 14 5.0 15 7.0	 µA µA µA µA µA µA	 VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

14.4 DC Characteristics: PIC16LV54A-02 (Commercial) PIC16LV54A-02 (Industrial)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –20°C ≤ TA ≤ +85°C (industrial)					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage XT, RC and LP options	VDD	 2.0	 —	 3.8	 V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) XT and RC(4) options LP option, Commercial LP option, Industrial	IDD	 — — —	 0.5 11 14	 — 27 35	 mA µA µA	 FOSC = 2.0 MHz, VDD = 3.0V FOSC = 32 kHz, VDD = 2.5V, WDT disabled FOSC = 32 kHz, VDD = 2.5V, WDT disabled
Power Down Current(5)(6) Commercial Industrial 	IPD	 — — — —	 2.5 0.25 3.5 0.3	 12 4.0 14 5.0	 µA µA µA µA	 VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

6: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection, if the SLEEP mode is entered or during initial power-up.

14.5 DC Characteristics: PIC16C54A-04, 10, 20, PIC16LC54A-04, PIC16LV54A-02 (Commercial) PIC16C54A-04I, 10I, 20I, PIC16LC54A-04I, PIC16LV54A-02I (Industrial) PIC16C54A-04E, 10E, 20E (Extended)

DC Characteristics All Pins Except Power Supply Pins	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ T_A ≤ +70°C (commercial) –40°C ≤ T_A ≤ +85°C (industrial) –20°C ≤ T_A ≤ +85°C (industrial - PIC16LV54A-02I) –40°C ≤ T_A ≤ +125°C (extended) Operating Voltage V_{DD} range is described in Section 14.1, Section 14.2 and Section 14.3.

Characteristic	Sym	Min	Typ(1)	Max	Units	Conditions
Input Low Voltage	V_{IL}					
I/O ports		V_{SS}	—	0.2 V_{DD}	V	Pin at hi-impedance
		V_{SS}	—	0.8V_{DD}	V	4.0V < V_{DD} ≤ 5.5V(5)
$\overline{MCLR}$ (Schmitt Trigger)		V_{SS}	—	0.15 V_{DD}	V	
T0CKI (Schmitt Trigger)		V_{SS}	—	0.15 V_{DD}	V	
OSC1 (Schmitt Trigger)		V_{SS}	—	0.15 V_{DD}	V	RC option only(4)
OSC1		V_{SS}	—	0.3 V_{DD}		XT, HS and LP options
Input High Voltage	V_{IH}					
I/O ports		0.2 V_{DD}+1V	—	V_{DD}	V	For all V_{DD}(5)
		2.0	—	V_{DD}	V	4.0V < V_{DD} ≤ 5.5V(5)
$\overline{MCLR}$ (Schmitt Trigger)		0.85 V_{DD}	—	V_{DD}	V	
T0CKI (Schmitt Trigger)		0.85 V_{DD}	—	V_{DD}	V	
OSC1 (Schmitt Trigger)		0.85 V_{DD}	—	V_{DD}	V	RC option only(4)
OSC1		0.7 V_{DD}	—	V_{DD}	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	V_{HYS}	0.15V_{DD}*	—	—	V	
Input Leakage Current(3)	I_{IL}					**For V_{DD} ≤ 5.5V**
I/O ports		-1.0	0.5	+1.0	µA	V_{SS} ≤ V_{PIN} ≤ V_{DD},
		—	—	—	—	Pin at hi-impedance
$\overline{MCLR}$		-5.0	—	+5.0	µA	V_{PIN} = V_{SS} +0.25V(2)
			0.5	+3.0	µA	V_{PIN} = V_{DD}(2)
T0CKI		-3.0	0.5	+3.0	µA	V_{SS} ≤ V_{PIN} ≤ V_{DD}
OSC1		-3.0	0.5	—	µA	V_{SS} ≤ V_{PIN} ≤ V_{DD}, XT, HS and LP options
Output Low Voltage	V_{OL}					
I/O ports		—	—	0.6	V	I_{OL} = 8.7 mA, V_{DD} = 4.5V
OSC2/CLKOUT		—	—	0.6	V	I_{OL} = 1.6 mA, V_{DD} = 4.5V, RC option only
Output High Voltage	V_{OH}					
I/O ports(3)		V_{DD}-0.7	—	—	V	I_{OH} = -5.4 mA, V_{DD} = 4.5V
OSC2/CLKOUT		V_{DD}-0.7	—	—	V	I_{OH} = -1.0 mA, V_{DD} = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the $\overline{MCLR}$/V_{PP} pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

14.6 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

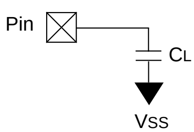
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 14-1: LOAD CONDITIONS - PIC16C54A



C_L = 50 pF for all pins except OSC2

15 pF for OSC2 in XT, HS or LP options when external clock is used to drive OSC1

14.7 Timing Diagrams and Specifications

FIGURE 14-2: EXTERNAL CLOCK TIMING - PIC16C54A

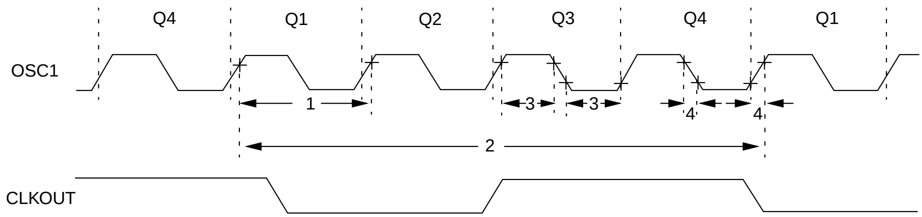


TABLE 14-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A

AC Characteristics — **Standard Operating Conditions (unless otherwise specified)**
Operating Temperature 0°C ≤ TA ≤ +70°C (commercial)
–40°C ≤ TA ≤ +85°C (industrial)
–20°C ≤ TA ≤ +85°C (industrial - PIC16LV54A-02I)
–40°C ≤ TA ≤ +125°C (extended)
Operating Voltage VDD range is described in Section 14.1, Section 14.2 and Section 14.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
	FOSC	External CLKIN Frequency(2)	DC	—	4.0	MHz	XT osc mode
			DC	—	2.0	MHz	XT osc mode (PIC16LV54A)
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	10	MHz	HS osc mode (10)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4.0	MHz	RC osc mode
			DC	—	2.0	MHz	RC osc mode (PIC16LV54A)
			0.1	—	4.0	MHz	XT osc mode
			0.1	—	2.0	MHz	XT osc mode (PIC16LV54A)
			4	—	4.0	MHz	HS osc mode (04)
			4	—	10	MHz	HS osc mode (10)
			4	—	20	MHz	HS osc mode (20)
			5	—	200	kHz	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

TABLE 14-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A (CON'T)

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –20°C ≤ TA ≤ +85°C (industrial - PIC16LV54A-02I) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 14.1, Section 14.2 and Section 14.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
1	TOSC	External CLKIN Period(2)	250	—	—	ns	XT osc mode
			500	—	—	ns	XT osc mode (PIC16LV54A)
			250	—	—	ns	HS osc mode (04)
			100	—	—	ns	HS osc mode (10)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	µs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			500	—	—	ns	RC osc mode (PIC16LV54A)
			250	—	10,000	ns	XT osc mode
			500	—	—	ns	XT osc mode (PIC16LV54A)
			250	—	250	ns	HS osc mode (04)
			100	—	250	ns	HS osc mode (10)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	µs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	µs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

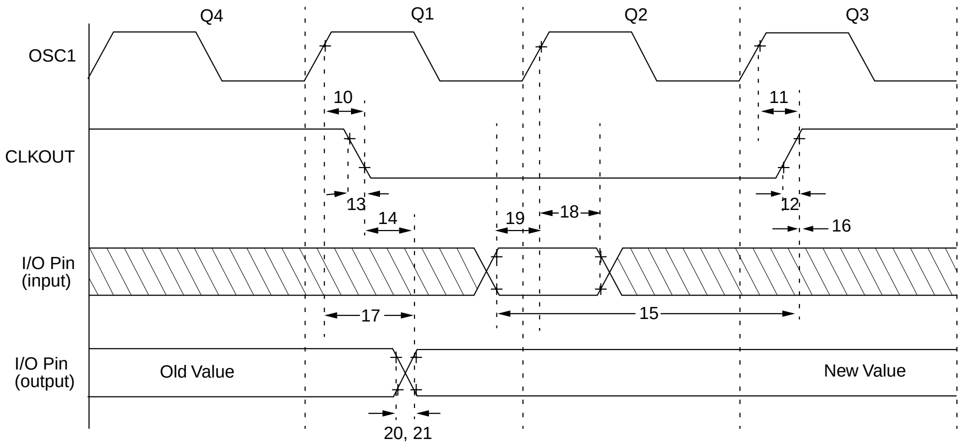
* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 14-3: CLKOUT AND I/O TIMING - PIC16C54A



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

TABLE 14-3: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54A

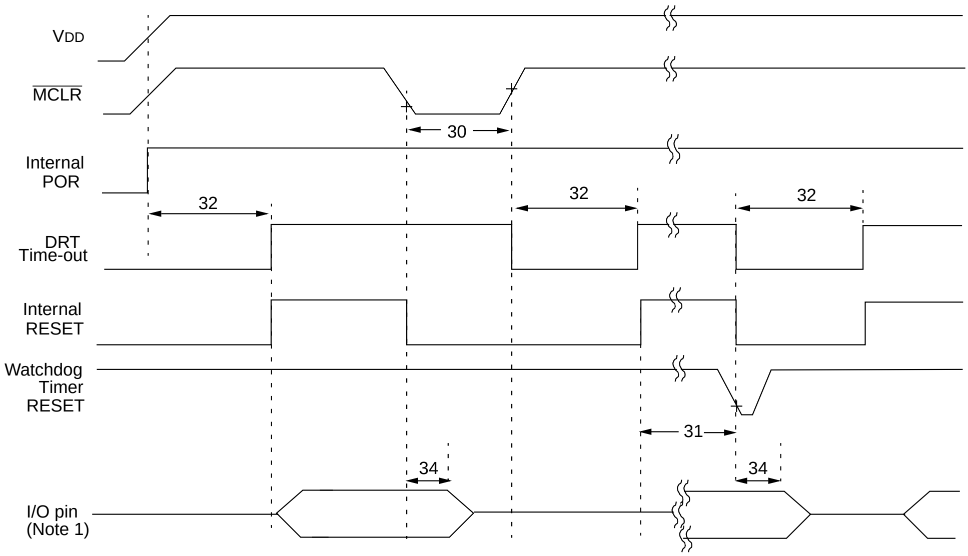
AC Characteristics — **Standard Operating Conditions (unless otherwise specified)**
Operating Temperature $0°C \leq T_A \leq +70°C$ (commercial)
$–40°C \leq T_A \leq +85°C$ (industrial)
$–20°C \leq T_A \leq +85°C$ (industrial - PIC16LV54A-02I)
$–40°C \leq T_A \leq +125°C$ (extended)
Operating Voltage VDD range is described in Section 14.1, Section 14.2 and Section 14.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time(2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.
** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.
3: See Figure 14-1 for loading conditions.

FIGURE 14-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54A



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 14-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54A

AC Characteristics **Standard Operating Conditions (unless otherwise specified)**
Operating Temperature 0°C ≤ TA ≤ +70°C (commercial)
–40°C ≤ TA ≤ +85°C (industrial)
–20°C ≤ TA ≤ +85°C (industrial - PIC16LV54A-02I)
–40°C ≤ TA ≤ +125°C (extended)
Operating Voltage VDD range is described in Section 14.1, Section 14.2 and Section 14.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	100* 1μs	— —	— —	ns —	VDD = 5.0V VDD = 5.0V (PIC16LV54A only)
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
34	Tioz	I/O Hi-impedance from MCLR Low	— —	— —	100* 1μs	ns —	 (PIC16LV54A only)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 14-5: TIMER0 CLOCK TIMINGS - PIC16C54A

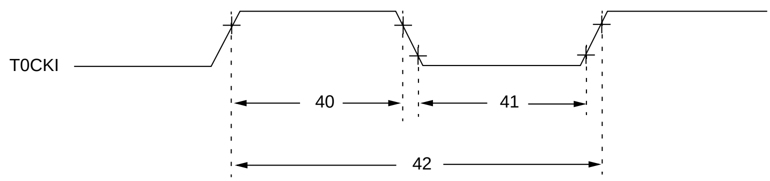


TABLE 14-5: TIMER0 CLOCK REQUIREMENTS - PIC16C54A

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –20°C ≤ TA ≤ +85°C (industrial - PIC16LV54A-02I) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 14.1, Section 14.2 and Section 14.3.					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or (TCY + 40)/N *	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NOTES:

15.0 ELECTRICAL CHARACTERISTICS - PIC16CR57B

Absolute Maximum Ratings†

Ambient Temperature under bias .... –55°C to +125°C
Storage Temperature .... –65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} .... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} .... 0 to +14V
Voltage on all other pins with respect to V_{SS} .... –0.6V to (V_{DD} + 0.6V)
Total Power Dissipation(1) .... 800 mW
Max. Current out of V_{SS} pin .... 150 mA
Max. Current into V_{DD} pin .... 100 mA
Max. Current into an input pin (T0CKI only) .... ±500 µA
Input Clamp Current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) .... ±20 mA
Output Clamp Current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) .... ±20 mA
Max. Output Current sunk by any I/O pin .... 25 mA
Max. Output Current sourced by any I/O pin .... 20 mA
Max. Output Current sourced by a single I/O port (PORTA, B or C) .... 50 mA
Max. Output Current sunk by a single I/O port (PORTA, B or C) .... 50 mA

Note 1: Power Dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

†NOTICE: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 15-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16CR57B-04	PIC16CR57B-10	PIC16CR57B-20	PIC16LCR57B-04
RC	VDD: 3.0V to 6.25V IDD: 2.5 mA max at 5.5V IPD: 4.0 µA max at 3.0V, WDT dis Freq: 4.0 MHz max	N/A	N/A	N/A
XT	VDD: 3.0V to 6.25V IDD: 2.5 mA max at 5.5V IPD: 4.0 µA max at 3.0V, WDT dis Freq: 4.0 MHz max	N/A	N/A	N/A
HS	N/A	VDD: 4.5V to 5.5V IDD: 10 mA max at 5.5V IPD: 4.0 µA max at 3.0V, WDT dis Freq: 10 MHz max	VDD: 4.5V to 5.5V IDD: 20 mA max at 5.5V IPD: 4.0 µA max at 3.0V, WDT dis Freq: 20 MHz max	N/A
LP	N/A	N/A	N/A	VDD: 2.5V to 6.25V IDD: 32 µA max at 32 kHz, 2.5V IPD: 4.0 µA max at 2.5V, WDT dis Freq: 200 kHz max

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

15.1 DC Characteristics: PIC16CR57B-04, 10, 20 (Commercial) PIC16CR57B-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \le T_A \le +70°C$ (commercial) $-40°C \le T_A \le +85°C$ (industrial)					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
RC and XT options		3.0	—	6.25	V	
HS option		4.5	—	5.5	V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
RC(4) and XT options		—	1.9	2.5	mA	FOSC = 4 MHz, VDD = 5.5V
HS option		—	2.5	8.0	mA	FOSC = 10 MHz, VDD = 5.5V
		—	4.7	17	mA	FOSC = 20 MHz, VDD = 5.5V
Power-Down Current(5)	IPD					
Commercial		—	4.0	12	μA	VDD = 3.0V, WDT enabled
		—	0.25	4.0	μA	VDD = 3.0V, WDT disabled
Industrial		—	4.0	14	μA	VDD = 3.0V, WDT enabled
		—	0.25	5.0	μA	VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

15.2 DC Characteristics: PIC16CR57B-04E, 10E, 20E (Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage RC and XT options HS options	V_{DD}	 3.25 4.5	 — —	 6.0 5.5	 V V	
RAM Data Retention Voltage(2)	V_{DR}	—	1.5*	—	V	Device in SLEEP mode
V_{DD} Start Voltage to ensure Power-on Reset	V_{POR}	—	V_{SS}	—	V	See Section 7.4 for details on Power-on Reset
V_{DD} Rise Rate to ensure Power-on Reset	S_{VDD}	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) RC(4) and XT options HS option 	I_{DD}	 — — —	 1.9 4.8 9.0	 3.3 10 20	 mA mA mA	 F_{OSC} = 4 MHz, V_{DD} = 5.5V F_{OSC} = 10 MHz, V_{DD} = 5.5V F_{OSC} = 20 MHz, V_{DD} = 5.5V
Power-Down Current(5)	I_{PD}	 — —	 5.0 0.8	 22 18	 μA μA	 V_{DD} = 3.25V, WDT enabled V_{DD} = 3.25V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{SS}, T0CKI = V_{DD}, $\overline{MCLR}$ = V_{DD}; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: I_R = V_{DD}/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} and V_{SS}.

15.3 DC Characteristics: PIC16LCR57B-04 (Commercial) PIC16LCR57B-04I (Industrial)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	2.5	—	6.25	V	LP option
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
Commercial		—	12	28	µA	FOSC = 32 kHz, VDD = 2.5V, WDT disabled
Industrial		—	15	37	µA	FOSC = 32 kHz, VDD = 2.5V, WDT disabled
Power-Down Current(5)	IPD					
Commercial			3.5	12	µA	VDD = 2.5V, WDT enabled
			0.2	4.0	µA	VDD = 2.5V, WDT disabled
Industrial			3.5	14	µA	VDD = 2.5V, WDT enabled
			0.2	5.0	µA	VDD = 2.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

15.4 DC Characteristics: PIC16CR57B-04, 10, 20, PIC16LCR57B-04 (Commercial) PIC16CR57B-04I, 10I, 20I, PIC16LCR57B-04I (Industrial)

DC Characteristics All Pins Except Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 15.1 and Section 15.3.					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		VSS	—	0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		VSS	—	0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS	—	0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS	—	0.15 VDD	V	RC option only(4)
OSC1		VSS	—	0.3 VDD	V	XT, HS and LP options
Input High Voltage	VIH					
I/O ports		0.45 VDD	—	VDD	V	For all VDD(5)
		2.0	—	VDD	V	4.0V < VDD ≤ 5.5V(5)
		0.36 VDD	—	VDD	V	VDD > 5.5V
MCLR (Schmitt Trigger)		0.85 VDD	—	VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD	—	VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD	—	VDD	V	RC option only(4)
OSC1		0.7 VDD	—	VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*	—	—	V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		–1.0		+1.0	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		–5.0	—	—	µA	VPIN = VSS + 0.25V(2)
			0.5	+5.0	µA	VPIN = VDD(2)
T0CKI		–3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
OSC1		–3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports		—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage(3)	VOH					
I/O ports		VDD –0.7	—	—	V	IOH = –5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD –0.7	—	—	V	IOH = –1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

15.5 DC Characteristics: PIC16CR57B-04E, 10E, 20E (Extended)

DC Characteristics All Pins Except Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C Operating Voltage VDD range is described in Section 15.2.					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		VSS	—	0.2 VDD	V	Pin at hi-impedance
$\overline{MCLR}$ (Schmitt Trigger)		VSS	—	0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS	—	0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS	—	0.15 VDD	V	RC option only(4)
OSC1		VSS	—	0.3 VDD	V	XT, HS and LP options
Input High Voltage	VIH					
I/O ports		0.45 VDD	—	VDD	V	For all VDD(5)
		2.0	—	VDD	V	4.0V < VDD ≤ 5.5V(5)
		0.36 VDD	—	VDD	V	VDD > 5.5V
$\overline{MCLR}$ (Schmitt Trigger)		0.85 VDD	—	VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD	—	VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD	—	VDD	V	RC option only(4)
OSC1		0.7 VDD	—	VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*	—	—	V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		–1.0	—	+1.0	μA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
$\overline{MCLR}$		–5.0	—	—	μA	VPIN = VSS + 0.25 V(2)
			0.5	+5.0	μA	VPIN = VDD(2)
T0CKI		–3.0	0.5	+3.0	μA	VSS ≤ VPIN ≤ VDD
OSC1		–3.0	0.5	+3.0	μA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports		—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage(3)	VOH					
I/O ports		VDD –0.7	—	—	V	IOH = –5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD –0.7	—	—	V	IOH = –1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

15.6 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

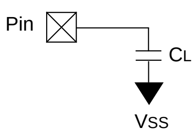
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 15-1: LOAD CONDITIONS



C_L = 50 pF for all pins except OSC2
15 pF for OSC2 in XT, HS or LP options when external clock is used to drive OSC1

15.7 Timing Diagrams and Specifications

FIGURE 15-2: EXTERNAL CLOCK TIMING - PIC16CR57B

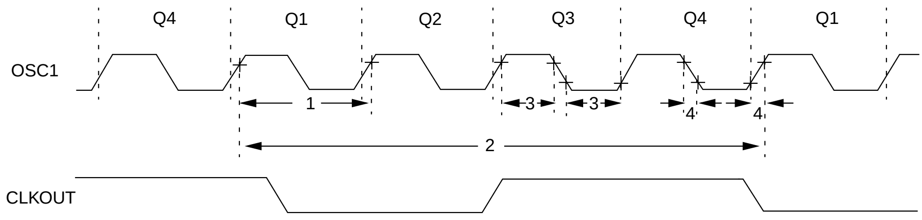


TABLE 15-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR57B

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 15.1, Section 15.2 and Section 15.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	FOSC	External CLKIN Frequency(2)	DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	10	MHz	HS osc mode (10)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4.0	MHz	RC osc mode
			0.1	—	4.0	MHz	XT osc mode
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	10	MHz	HS osc mode (10)
			4.0	—	20	MHz	HS osc mode (20)
			5.0	—	200	kHz	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

TABLE 15-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR57B (CON'T)

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 15.1, Section 15.2 and Section 15.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
1	TOSC	External CLKIN Period(2)	250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			100	—	—	ns	HS osc mode (10)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	µs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			100	—	250	ns	HS osc mode (10)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	µs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	µs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

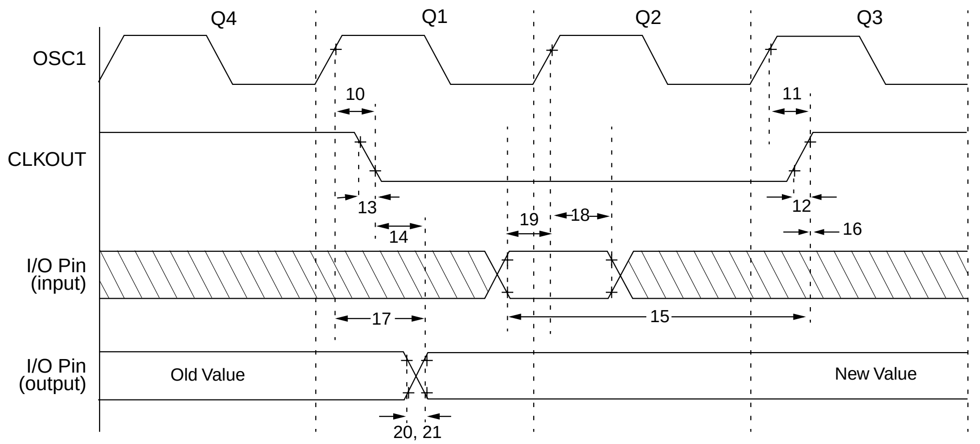
* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 15-3: CLKOUT AND I/O TIMING - PIC16CR57B



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

TABLE 15-3: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR57B

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ T_A ≤ +70°C (commercial) –40°C ≤ T_A ≤ +85°C (industrial) –40°C ≤ T_A ≤ +125°C (extended) Operating Voltage V_{DD} range is described in Section 15.1, Section 15.2 and Section 15.3.					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time(2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 T_{CY}+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

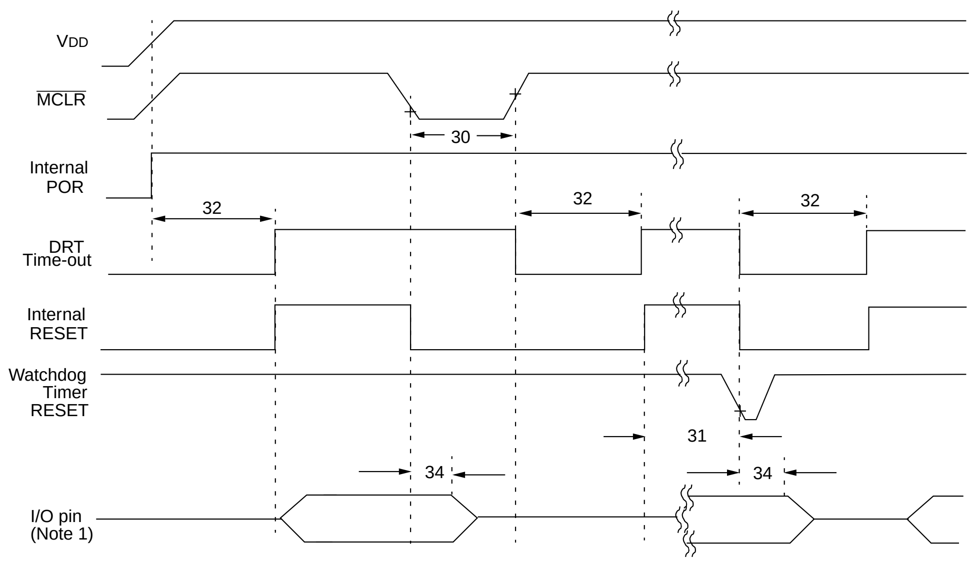
** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x T_{OSC}.

3: See Figure 15-1 for loading conditions.

FIGURE 15-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR57B



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 15-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR57B

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 15.1, Section 15.2 and Section 15.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	1.0*	—	—	µs	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
34	Tioz	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low	—	—	1.0*	µs	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-5: TIMER0 CLOCK TIMINGS - PIC16CR57B

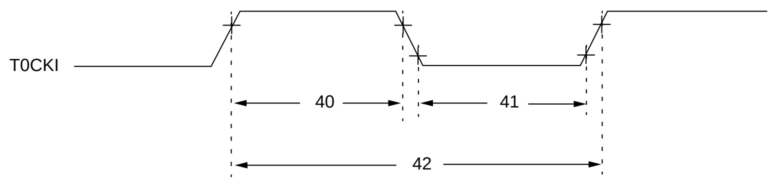


TABLE 15-5: TIMER0 CLOCK REQUIREMENTS - PIC16CR57B

AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 15.1, Section 15.2 and Section 15.3.				
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or (TCY + 40)/N*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NOTES:

16.0 ELECTRICAL CHARACTERISTICS - PIC16C58A

Absolute Maximum Ratings†

Ambient Temperature under bias .... –55°C to +125°C
Storage Temperature .... –65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} .... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} .... 0 to +14V
Voltage on all other pins with respect to V_{SS} .... –0.6V to (V_{DD} + 0.6V)
Total Power Dissipation(1) .... 800 mW
Max. Current out of V_{SS} pin .... 150 mA
Max. Current into V_{DD} pin .... 100 mA
Max. Current into an input pin (T0CKI only) .... ±500 μA
Input Clamp Current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) .... ±20 mA
Output Clamp Current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) .... ±20 mA
Max. Output Current sunk by any I/O pin .... 25 mA
Max. Output Current sourced by any I/O pin .... 20 mA
Max. Output Current sourced by a single I/O port (PORTA or B) .... 50 mA
Max. Output Current sunk by a single I/O port (PORTA or B) .... 50 mA

Note 1: Power Dissipation is calculated as follows: Pdis = $V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 16-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C58A-04	PIC16C58A-10	PIC16C58A-20	PIC16LC58A-04
RC	VDD: 3.0V to 6.25V IDD: 2.5 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 0.5 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.
XT	VDD: 3.0V to 6.25V IDD 2.5 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 0.5 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.
HS	N/A	VDD: 4.5V to 5.5V IDD: 8.0 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 17 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 20 MHz max.	N/A
LP	VDD: 3.0V to 6.25V IDD: 15 μA typ. at 32kHz, 3.0V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 200 kHz max.	N/A	N/A	VDD: 2.5V to 6.25V IDD: 28 μA max. at 32kHz, 2.5V WDT dis IPD: 4.0 μA max. at 2.5V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

OSC	PIC16C58A/JW	PIC16LV58A-02
RC	VDD: 3.0V to 6.25V IDD: 2.5 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 2.0V to 3.8V IDD: 0.5 mA typ. at 3.0V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 2.0 MHz max.
XT	VDD: 3.0V to 6.25V IDD 2.5 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 2.0V to 3.8V IDD: 0.5 mA typ. at 3.0V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 2.0 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 17 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 20 MHz max.	N/A
LP	VDD: 2.5V to 6.25V IDD: 28 μA max. at 32kHz, 2.5V WDT dis IPD: 4.0 μA max. at 2.5V WDT dis Freq: 200 kHz max.	VDD: 2.0V to 3.8V IDD: 27 μA max. at 32kHz, 2.5V WDT dis IPD: 4.0 μA max. at 2.5V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

16.1 DC Characteristics: PIC16C58A-04, 10, 20 (Commercial) PIC16C58A-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage XT, RC and LP options HS option	VDD	 3.0 4.5	 — —	 6.25 5.5	 V V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) XT and RC(4) options HS option LP option, Commercial LP option, Industrial	IDD	 — — — — —	 1.9 2.5 4.7 15 18	 2.5 8.0 17 31 39	 mA mA mA μA μA	 FOSC = 4.0 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 20 MHz, VDD = 5.5V FOSC = 32 kHz, VDD = 3.0V, WDT disabled FOSC = 32 kHz, VDD = 3.0V, WDT disabled
Power Down Current(5) Commercial Industrial 	IPD	 — — — —	 4.0 0.25 5.0 0.3	 12 4.0 14 5.0	 μA μA μA μA	 VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

16.2 DC Characteristics: PIC16C58A-04E, 10E, 20E (Extended)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ T_A ≤ +125°C (extended)					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	V_{DD}					
XT and RC options		3.5	—	5.5	V	
HS option		4.5	—	5.5	V	
RAM Data Retention Voltage(2)	V_{DR}	—	1.5*	—	V	Device in SLEEP mode
V_{DD} start voltage to ensure Power-On Reset	V_{POR}	—	V_{SS}	—	V	See Section 7.4 for details on Power-on Reset
V_{DD} rise rate to ensure Power-On Reset	S_{VDD}	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	I_{DD}					
XT and RC(4) options		—	1.9	3.3	mA	F_{OSC} = 4.0 MHz, V_{DD} = 5.5V
HS option		—	4.8	10	mA	F_{OSC} = 10 MHz, V_{DD} = 5.5V
		—	9.0	20	mA	F_{OSC} = 20 MHz, V_{DD} = 5.5V
Power Down Current(5)	I_{PD}					
XT and RC options		—	5.0	22	μA	V_{DD} = 3.5V, WDT enabled
		—	0.8	18	μA	V_{DD} = 3.5V, WDT disabled
HS option		—	4.0	22	μA	V_{DD} = 3.5V, WDT enabled
		—	0.25	18	μA	V_{DD} = 3.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{SS}, T0CKI = V_{DD}, $\overline{MCLR}$ = V_{DD}; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2Rext$ (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} and V_{SS}.

16.3 DC Characteristics: PIC16LC58A-04 (Commercial) PIC16LC58A-04I (Industrial) PIC16LC58A-04 (Extended)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended)					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage XT, RC and LP options	VDD	 2.5	 —	 6.25	 V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) XT and RC(4) options LP option, Commercial LP option, Industrial LP option, Extended	IDD	 — — — —	 0.5 12 12 12	 2.5 27 35 37	 mA µA µA µA	 FOSC = 4.0 MHz, VDD = 5.5V FOSC = 32 kHz, VDD = 2.5V WDT disabled FOSC = 32 kHz, VDD = 2.5V WDT disabled FOSC = 32 kHz, VDD = 2.5V WDT disabled
Power Down Current(5) Commercial Industrial Extended 	IPD	 — — — — — —	 2.5 0.25 2.5 0.25 2.5 0.25	 12 4.0 14 5.0 15 7.0	 µA µA µA µA µA µA	 VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

16.4 DC Characteristics: PIC16LV58A-02 (Commercial) PIC16LV58A-02 (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –20°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage XT, RC and LP options	VDD	 2.0	 —	 3.8	 V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See section on Power-On Reset for details
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See section on Power-On Reset for details
Supply Current(3) XT and RC(4) options LP option, Commercial LP option, Industrial	IDD	 — — —	 0.5 11 14	 1.8 27 35	 mA µA µA	 FOSC = 2.0 MHz, VDD = 3.0V FOSC = 32 kHz, VDD = 2.5V, WDT disabled FOSC = 32 kHz, VDD = 2.5V, WDT disabled
Power Down Current(5)(6) Commercial Industrial 	IPD	 — — — —	 2.5 0.25 2.5 0.25	 12 4.0 14 5.0	 µA µA µA µA	 VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

6: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection, if the SLEEP mode is entered or during initial power-up.

16.5 DC Characteristics: PIC16C58A-04, 10, 20, PIC16LC58A-04, PIC16LV58A-02 (Commercial) PIC16C58A-04I, 10I, 20I, PIC16LC58A-04I, PIC16LV58A-02I (Industrial) PIC16C58A-04E, 10E, 20E (Extended)

DC Characteristics All Pins Except Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \le T_A \le +70°C$ (commercial) $–40°C \le T_A \le +85°C$ (industrial) $–20°C \le T_A \le +85°C$ (industrial - PIC16LV58A) $–40°C \le T_A \le +125°C$ (extended) Operating Voltage VDD range is described in Section 16.1, Section 16.2 and Section 16.3.

Characteristic	Sym	Min	Typ(1)	Max	Units	Conditions
Input Low Voltage	VIL					
I/O ports		VSS	—	0.2 VDD	V	Pin at hi-impedance
$\overline{MCLR}$ (Schmitt Trigger)		VSS	—	0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS	—	0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS	—	0.15 VDD	V	RC option only(4)
OSC1		VSS	—	0.3 VDD	V	XT, HS and LP options
Input High Voltage	VIH					
I/O ports		0.2 VDD+1V	—	VDD	V	For all VDD(5)
		2.0	—	VDD	V	4.0V < VDD ≤ 5.5V(5)
$\overline{MCLR}$ (Schmitt Trigger)		0.85 VDD	—	VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD	—	VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD	—	VDD	V	RC option only(4)
OSC1		0.7 VDD	—	VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*	—	—	V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		-1.0	0.5	+1.0	μA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
$\overline{MCLR}$		-5.0	—	—	μA	VPIN = VSS +0.25V(2)
			0.5	+5.0	μA	VPIN = VDD(2)
T0CKI		-3.0	0.5	+3.0	μA	VSS ≤ VPIN ≤ VDD
OSC1		-3.0	0.5	+3.0	μA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports		—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage	VOH					
I/O ports(3)		VDD-0.7	—	—	V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD-0.7	—	—	V	IOH = -1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the $\overline{MCLR}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

16.6 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

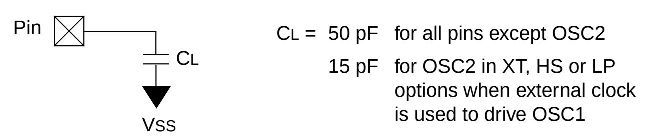
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 16-1: LOAD CONDITIONS - PIC16C58A



16.7 Timing Diagrams and Specifications

FIGURE 16-2: EXTERNAL CLOCK TIMING - PIC16C58A

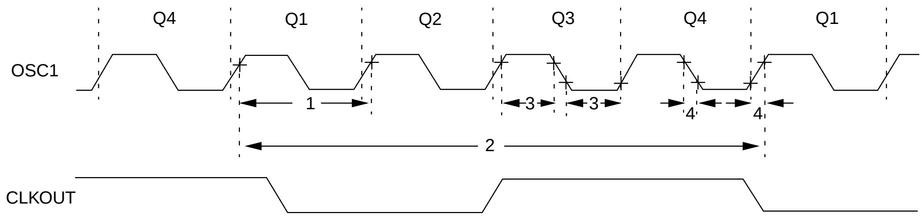


TABLE 16-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C58A

AC Characteristics — **Standard Operating Conditions (unless otherwise specified)**
Operating Temperature $0°C \le T_A \le +70°C$ (commercial)
$-40°C \le T_A \le +85°C$ (industrial)
$-20°C \le T_A \le +85°C$ (industrial - PIC16LV58A)
$-40°C \le T_A \le +125°C$ (extended)
Operating Voltage VDD range is described in Section 16.1, Section 16.2 and Section 16.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
	FOSC	External CLKIN Frequency(2)	DC	—	4.0	MHz	XT osc mode
			DC	—	2.0	MHz	XT osc mode (PIC16LV58A)
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	10	MHz	HS osc mode (10)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4.0	MHz	RC osc mode
			DC	—	2.0	MHz	RC osc mode (PIC16LV58A)
			0.1	—	4.0	MHz	XT osc mode
			0.1	—	2.0	MHz	XT osc mode (PIC16LV58A)
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	10	MHz	HS osc mode (10)
			4.0	—	20	MHz	HS osc mode (20)
			5.0	—	200	kHz	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

TABLE 16-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C58A (CON'T)

AC Characteristics — **Standard Operating Conditions (unless otherwise specified)**
Operating Temperature 0°C ≤ TA ≤ +70°C (commercial)
–40°C ≤ TA ≤ +85°C (industrial)
–20°C ≤ TA ≤ +85°C (industrial - PIC16LV58A)
–40°C ≤ TA ≤ +125°C (extended)
Operating Voltage VDD range is described in Section 16.1, Section 16.2 and Section 16.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
1	TOSC	External CLKIN Period(2)	250	—	—	ns	XT osc mode
			500	—	—	ns	XT osc mode (PIC16LV58A)
			250	—	—	ns	HS osc mode (04)
			100	—	—	ns	HS osc mode (10)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	µs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			500	—	—	ns	RC osc mode (PIC16LV58A)
			250	—	10,000	ns	XT osc mode
			500	—	—	ns	XT osc mode (PIC16LV58A)
			250	—	250	ns	HS osc mode (04)
			100	—	250	ns	HS osc mode (10)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	µs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	µs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

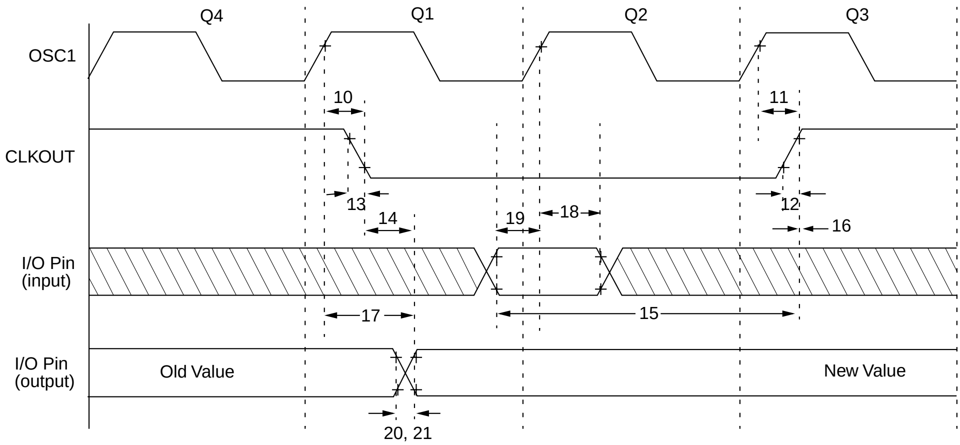
* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 16-3: CLKOUT AND I/O TIMING - PIC16C58A



Note: Refer to Figure 16-1 for load conditions.

TABLE 16-3: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C58A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –20°C ≤ TA ≤ +85°C (industrial - PIC16LV58A) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 16.1, Section 16.2 and Section 16.3.					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5	15**	ns
13	TckF	CLKOUT fall time(2)	—	5	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

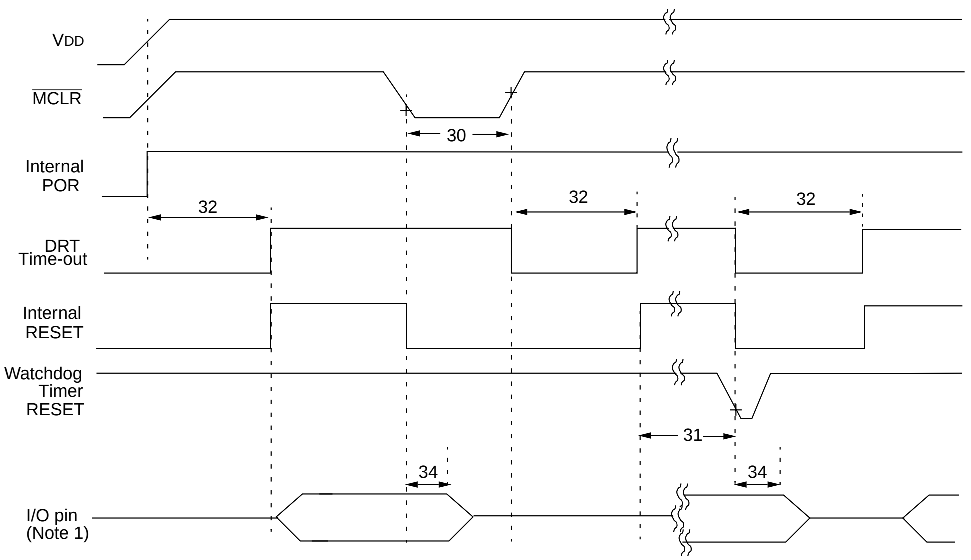
** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25˚C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 16-1 for loading conditions.

FIGURE 16-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C58A



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 16-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C58A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \le T_A \le +70°C$ (commercial) $-40°C \le T_A \le +85°C$ (industrial) $-20°C \le T_A \le +85°C$ (industrial - PIC16LV58A) $-40°C \le T_A \le +125°C$ (extended) Operating Voltage VDD range is described in Section 16.1, Section 16.2 and Section 16.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	100* 1µs	— —	— —	ns —	VDD = 5.0V VDD = 5.0V (PIC16LV58A only)
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
34	Tioz	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low	— —	— —	100* 1µs	ns —	 (PIC16LV58A only)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 16-5: TIMER0 CLOCK TIMINGS - PIC16C58A

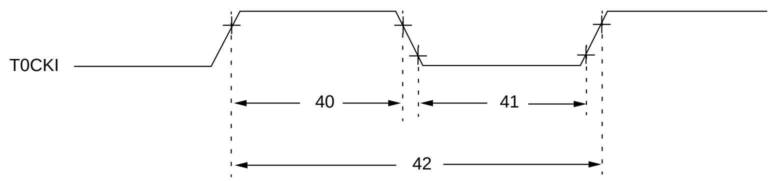


TABLE 16-5: TIMER0 CLOCK REQUIREMENTS - PIC16C58A

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –20°C ≤ TA ≤ +85°C (industrial - PIC16LV58A) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 16.1, Section 16.2 and Section 16.3.					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{TCY + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NOTES:

17.0 ELECTRICAL CHARACTERISTICS - PIC16CR58A

Absolute Maximum Ratings†

Ambient Temperature under bias .... –55°C to +125°C
Storage Temperature .... –65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} .... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} .... 0 to +14V
Voltage on all other pins with respect to V_{SS} .... –0.6V to (V_{DD} + 0.6V)
Total Power Dissipation(1) .... 800 mW
Max. Current out of V_{SS} pin .... 150 mA
Max. Current into V_{DD} pin .... 100 mA
Max. Current into an input pin (T0CKI only) .... ±500 µA
Input Clamp Current, I_{IK} (V_I < 0 or V_I > V_{DD}) .... ±20 mA
Output Clamp Current, I_{OK} (V_O < 0 or V_O > V_{DD}) .... ±20 mA
Max. Output Current sunk by any I/O pin .... 25 mA
Max. Output Current sourced by any I/O pin .... 20 mA
Max. Output Current sourced by a single I/O port (PORTA or B) .... 50 mA
Max. Output Current sunk by a single I/O port (PORTA or B) .... 50 mA

Note 1: Power Dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 17-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16CR58A-04	PIC16CR58A-10	PIC16CR58A-20	PIC16LCR58A-04
RC	V_{DD}: 3.0V to 6.25V I_{DD}: 2.5 mA max at 5.5V I_{PD}: 4.0 μA max at 3.0V, WDT dis Freq: 4.0 MHz max	N/A	N/A	N/A
XT	V_{DD}: 3.0V to 6.25V I_{DD}: 2.5 mA max at 5.5V I_{PD}: 4.0 μA max at 3.0V, WDT dis Freq: 4.0 MHz max	N/A	N/A	N/A
HS	N/A	V_{DD}: 4.5V to 5.5V I_{DD}: 8.0 mA max at 5.5V I_{PD}: 4.0 μA max at 3.0V, WDT dis Freq: 10 MHz max	V_{DD}: 4.5V to 5.5V I_{DD}: 17 mA max at 5.5V I_{PD}: 4.0 μA max at 3.0V, WDT dis Freq: 20 MHz max	N/A
LP	N/A	N/A	N/A	V_{DD}: 2.5V to 6.25V I_{DD}: 28 μA max at 32 kHz, 2.5V I_{PD}: 4.0 μA max at 2.5V, WDT dis Freq: 200 kHz max

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

17.1 DC Characteristics: PIC16CR58A-04, 10, 20 (Commercial) PIC16CR58A-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \le T_A \le +70°C$ (commercial) $-40°C \le T_A \le +85°C$ (industrial)					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage RC and XT options HS option	VDD	 3.0 4.5	 — —	 6.25 5.5	 V V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) RC(4) and XT options HS option 	IDD	 — — —	 1.9 2.5 4.7	 2.5 8.0 17	 mA mA mA	 FOSC = 4.0 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 20 MHz, VDD = 5.5V
Power-Down Current(5) Commercial Industrial 	IPD	 — — — —	 4.0 0.25 4.0 0.25	 12 4.0 14 5.0	 μA μA μA μA	 VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

17.2 DC Characteristics: PIC16CR58A-04E, 10E, 20E (Extended)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (extended)					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage RC and XT options HS options	VDD	 3.25 4.5	 — —	 6.0 5.5	 V V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) RC(4) and XT options HS option	IDD	 — — —	 1.9 4.8 9.0	 3.3 10 20	 mA mA mA	 FOSC = 4.0 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 20 MHz, VDD = 5.5V
Power-Down Current(5)	IPD	 — —	 5.0 0.8	 22 18	 μA μA	 VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

17.3 DC Characteristics: PIC16LCR58A-04 (Commercial) PIC16LCR58A-04I (Industrial)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	2.5	—	6.25	V	LP option
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
Commercial		—	12	28	µA	FOSC = 32 kHz, VDD = 2.5V, WDT disabled
Industrial		—	15	37	µA	FOSC = 32 kHz, VDD = 2.5V, WDT disabled
Power-Down Current(5)	IPD					
Commercial		—	3.5	12	µA	VDD = 2.5V, WDT enabled
		—	0.2	4.0	µA	VDD = 2.5V, WDT disabled
Industrial		—	3.5	14	µA	VDD = 2.5V, WDT enabled
		—	0.2	5.0	µA	VDD = 2.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

17.4 DC Characteristics: PIC16CR58A-04, 10, 20, PIC16LCR58A-04 (Commercial) PIC16CR58A-04I, 10I, 20I, PIC16LCR58A-04I (Industrial)

DC Characteristics All Pins Except Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 17.1 and Section 17.3.					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		VSS	—	0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		VSS	—	0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS	—	0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS	—	0.15 VDD	V	RC option only(4)
OSC1		VSS	—	0.3 VDD	V	XT, HS and LP options
Input High Voltage	VIH					
I/O ports		0.45 VDD	—	VDD	V	For all VDD(5)
		2.0	—	VDD	V	4.0V < VDD ≤ 5.5V(5)
		0.36 VDD	—	VDD	V	VDD > 5.5V
MCLR (Schmitt Trigger)		0.85 VDD	—	VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD	—	VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD	—	VDD	V	RC option only(4)
OSC1		0.7 VDD	—	VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*	—	—	V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		–1.0	—	+1.0	μA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		–5.0	—	—	μA	VPIN = VSS + 0.25V(2)
			0.5	+5.0	μA	VPIN = VDD(2)
T0CKI		–3.0	0.5	+3.0	μA	VSS ≤ VPIN ≤ VDD
OSC1		–3.0	0.5	+3.0	μA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports		—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage(3)	VOH					
I/O ports		VDD –0.7	—	—	V	IOH = –5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD –0.7	—	—	V	IOH = –1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

 Preliminary

17.5 DC Characteristics: PIC16CR58A-04E, 10E, 20E (Extended)

DC Characteristics All Pins Except Power Supply Pins						**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended) Operating Voltage V_{DD} range is described in Section 17.2.
Characteristic	**Sym**	**Min**	**Typ[(1)]**	**Max**	**Units**	**Conditions**
Input Low Voltage	V_{IL}					
I/O ports		V_{SS}	—	0.2 V_{DD}	V	Pin at hi-impedance
$\overline{MCLR}$ (Schmitt Trigger)		V_{SS}	—	0.15 V_{DD}	V	
T0CKI (Schmitt Trigger)		V_{SS}	—	0.15 V_{DD}	V	
OSC1 (Schmitt Trigger)		V_{SS}	—	0.15 V_{DD}	V	RC option only[(4)]
OSC1		V_{SS}	—	0.3 V_{DD}	V	XT, HS and LP options
Input High Voltage	V_{IH}					
I/O ports		0.45 V_{DD}	—	V_{DD}	V	For all V_{DD}[(5)]
		2.0	—	V_{DD}	V	4.0V < V_{DD} ≤ 5.5V[(5)]
		0.36 V_{DD}	—	V_{DD}	V	V_{DD} > 5.5V
$\overline{MCLR}$ (Schmitt Trigger)		0.85 V_{DD}	—	V_{DD}	V	
T0CKI (Schmitt Trigger)		0.85 V_{DD}	—	V_{DD}	V	
OSC1 (Schmitt Trigger)		0.85 V_{DD}	—	V_{DD}	V	RC option only[(4)]
OSC1		0.7 V_{DD}	—	V_{DD}	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	V_{HYS}	0.15V_{DD}*	—	—	V	
Input Leakage Current[(3)]	I_{IL}					**For V_{DD} ≤ 5.5V**
I/O ports		–1.0	—	+1.0	μA	V_{SS} ≤ V_{PIN} ≤ V_{DD}, Pin at hi-impedance
$\overline{MCLR}$		–5.0	—	—	μA	V_{PIN} = V_{SS} + 0.25V[(2)]
			0.5	+5.0	μA	V_{PIN} = V_{DD}[(2)]
T0CKI		–3.0	0.5	+3.0	μA	V_{SS} ≤ V_{PIN} ≤ V_{DD}
OSC1		–3.0	0.5	+3.0	μA	V_{SS} ≤ V_{PIN} ≤ V_{DD}, XT, HS and LP options
Output Low Voltage	V_{OL}					
I/O ports		—	—	0.6	V	I_{OL} = 8.7 mA, V_{DD} = 4.5V
OSC2/CLKOUT		—	—	0.6	V	I_{OL} = 1.6 mA, V_{DD} = 4.5V, RC option only
Output High Voltage[(3)]	V_{OH}					
I/O ports		V_{DD} –0.7	—	—	V	I_{OH} = –5.4 mA, V_{DD} = 4.5V
OSC2/CLKOUT		V_{DD} –0.7	—	—	V	I_{OH} = –1.0 mA, V_{DD} = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the $\overline{MCLR}$/V_{PP} pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

17.6 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

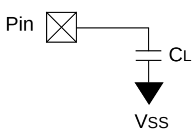
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 17-1: LOAD CONDITIONS - PIC16CR58A



C_L = 50 pF for all pins except OSC2

15 pF for OSC2 in XT, HS or LP options when external clock is used to drive OSC1

17.7 Timing Diagrams and Specifications

FIGURE 17-2: EXTERNAL CLOCK TIMING - PIC16CR58A

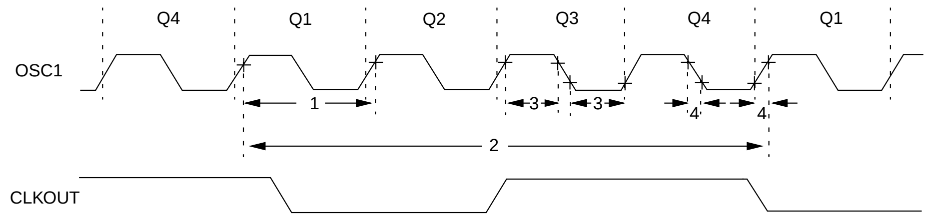


TABLE 17-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR58A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 17.1, Section 17.2 and Section 17.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	FOSC	External CLKIN Frequency(2)	DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	10	MHz	HS osc mode (10)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4.0	MHz	RC osc mode
			0.1	—	4.0	MHz	XT osc mode
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	10	MHz	HS osc mode (10)
			4.0	—	20	MHz	HS osc mode (20)
			5.0	—	200	kHz	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

TABLE 17-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR58A (CON'T)

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 17.1, Section 17.2 and Section 17.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
1	TOSC	External CLKIN Period(2)	250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			100	—	—	ns	HS osc mode (10)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	μs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			100	—	250	ns	HS osc mode (10)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	μs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

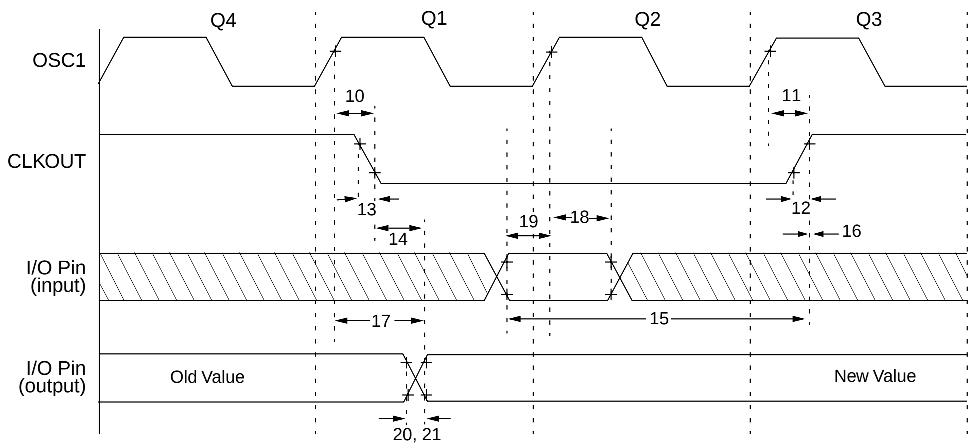
* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 17-3: CLKOUT AND I/O TIMING - PIC16CR58A



Note: Refer to Figure 17-1 for load conditions.

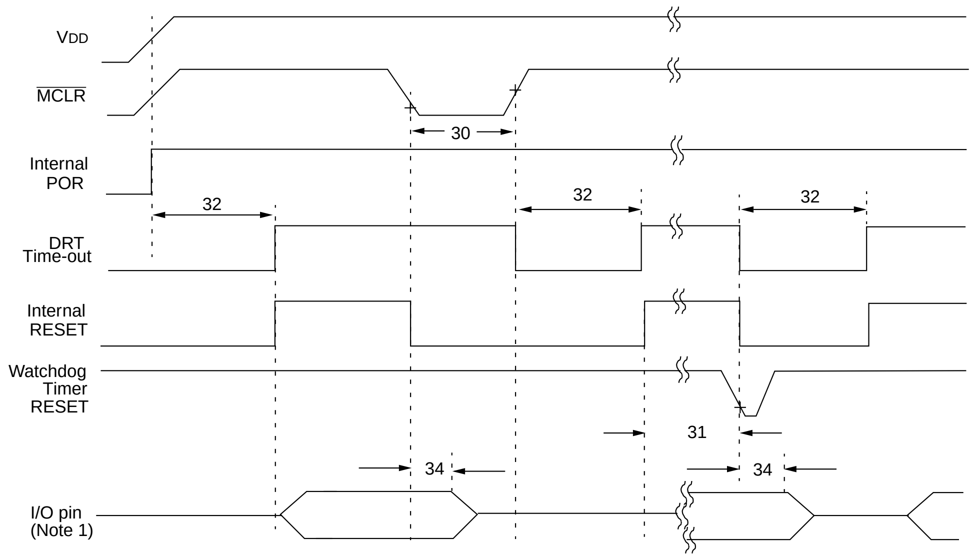
TABLE 17-3: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR58A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 17.1, Section 17.2 and Section 17.3.					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time(2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.
** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.
3: See Figure 17-1 for loading conditions.

FIGURE 17-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR58A



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 17-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR58A

AC Characteristics **Standard Operating Conditions (unless otherwise specified)**
Operating Temperature 0°C ≤ TA ≤ +70°C (commercial)
–40°C ≤ TA ≤ +85°C (industrial)
–40°C ≤ TA ≤ +125°C (extended)
Operating Voltage VDD range is described in Section 17.1, Section 17.2 and Section 17.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	1.0*	—	—	µs	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
34	Tioz	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low	—	—	1.0*	µs	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 17-5: TIMER0 CLOCK TIMINGS - PIC16CR58A

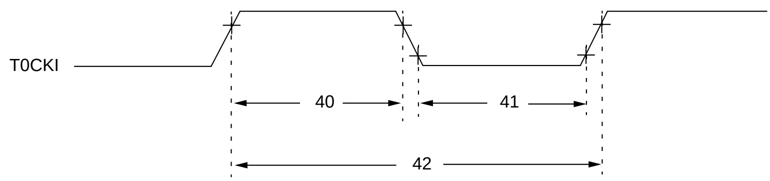


TABLE 17-5: TIMER0 CLOCK REQUIREMENTS - PIC16CR58A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature $0°C \le T_A \le +70°C$ (commercial) $-40°C \le T_A \le +85°C$ (industrial) $-40°C \le T_A \le +125°C$ (extended) Operating Voltage VDD range is described in Section 17.1, Section 17.2 and Section 17.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NOTES:

18.0 DC AND AC CHARACTERISTICS - PIC16C54A/CR57B/C58A/CR58A

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean – 3σ) respectively, where σ is standard deviation.

FIGURE 18-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

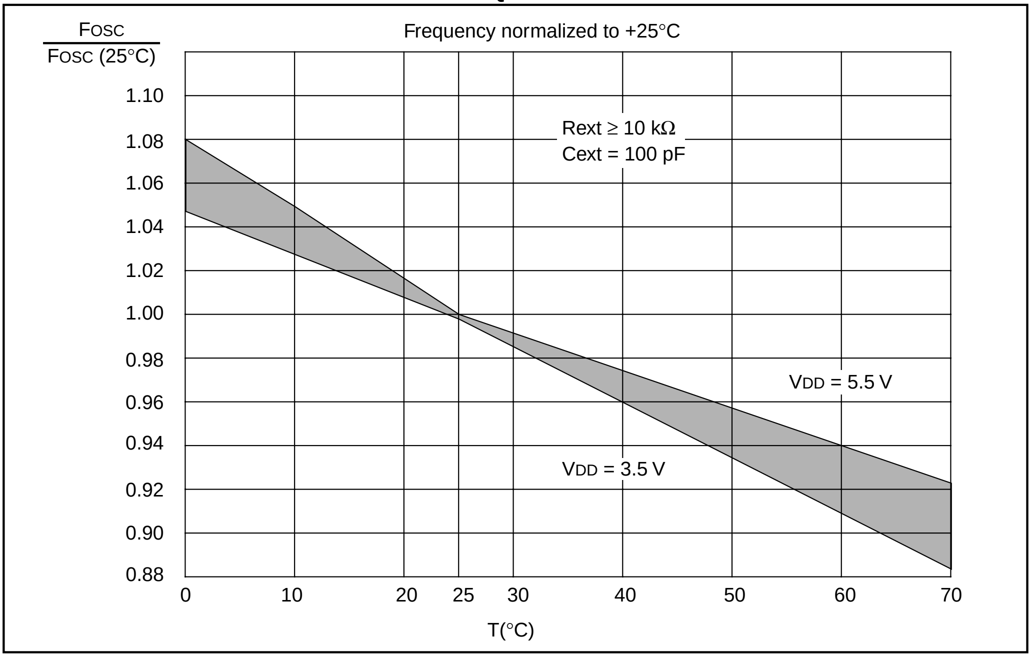


TABLE 18-1: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5 V, 25°C	
20 pF	3.3 k	4.973 MHz	± 27%
	5 k	3.82 MHz	± 21%
	10 k	2.22 MHz	± 21%
	100 k	262.15 kHz	± 31%
100 pF	3.3 k	1.63 MHz	± 13%
	5 k	1.19 MHz	± 13%
	10 k	684.64 kHz	± 18%
	100 k	71.56 kHz	± 25%
300 pF	3.3 k	660 kHz	± 10%
	5.0 k	484.1 kHz	± 14%
	10 k	267.63 kHz	± 15%
	160 k	29.44 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5 V.

FIGURE 18-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF

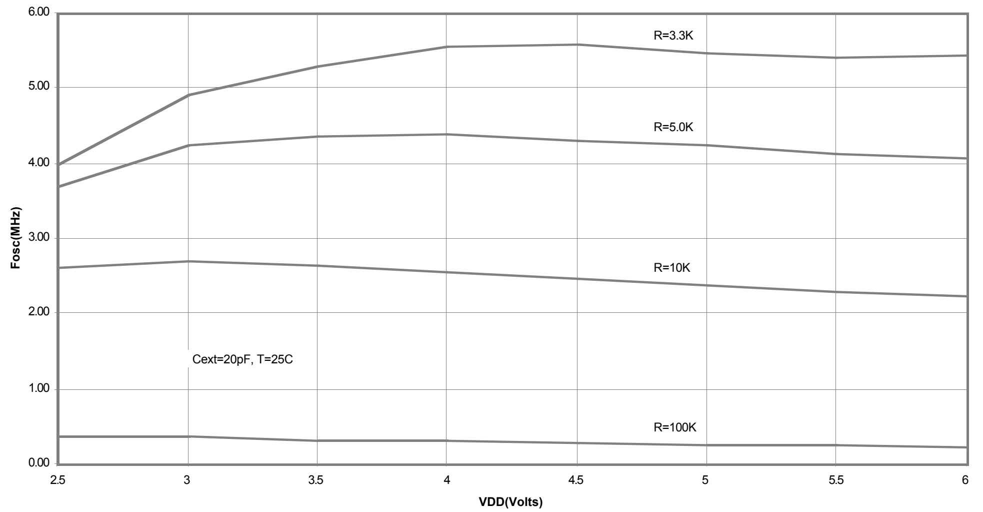


FIGURE 18-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF

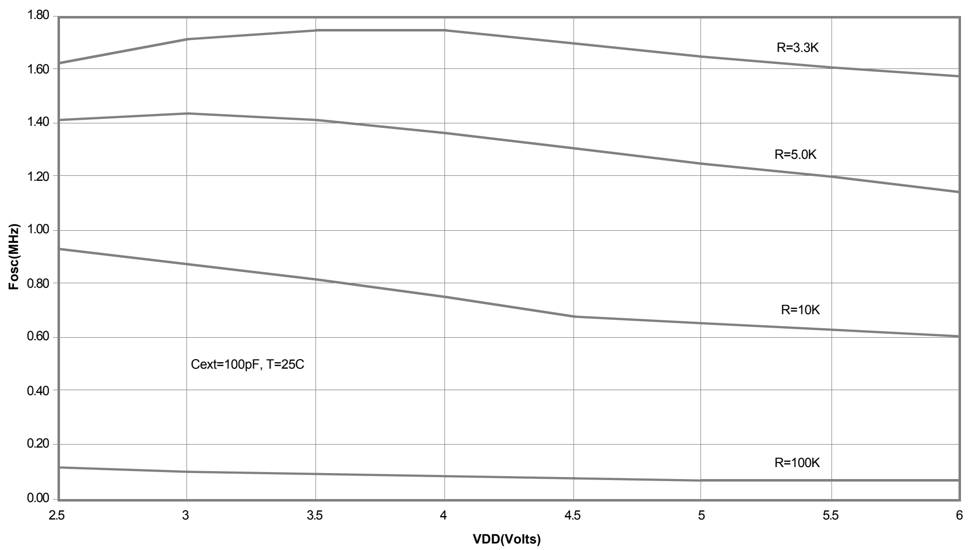


FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF

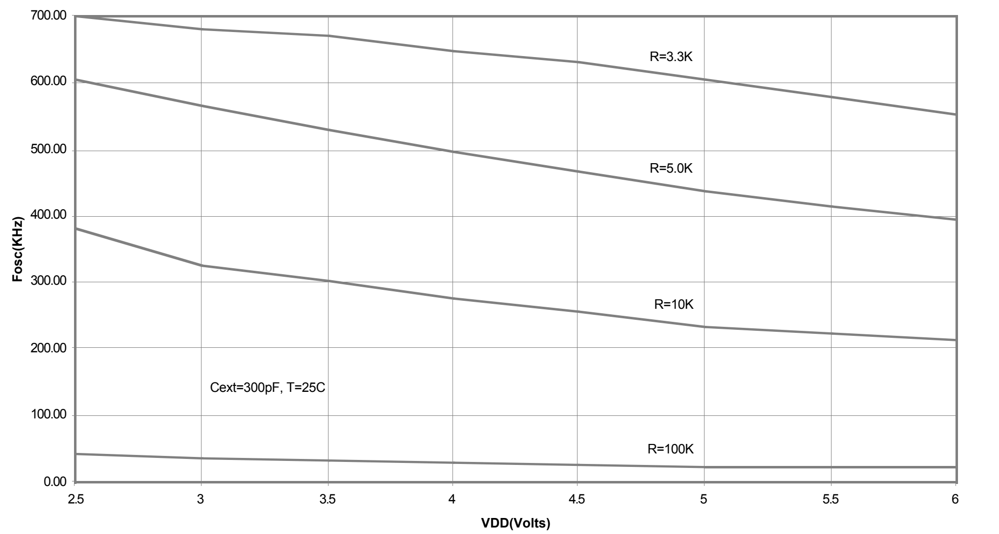


FIGURE 18-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)

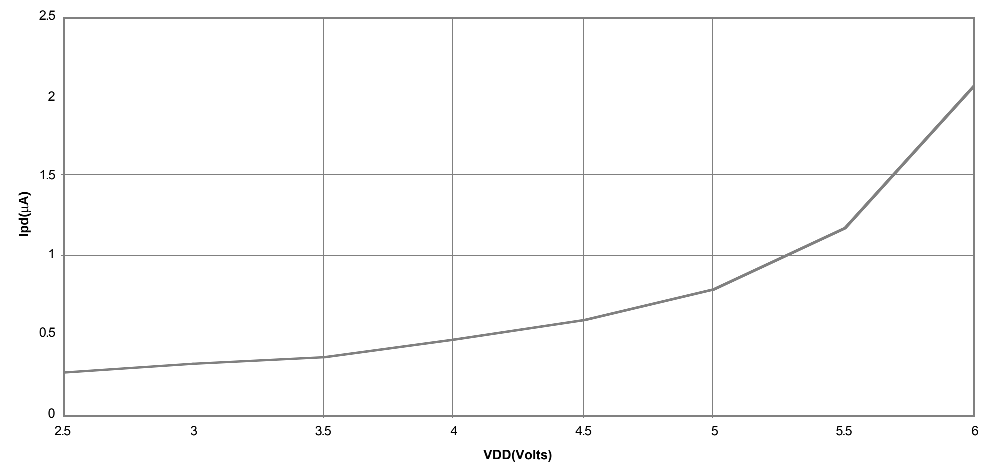


FIGURE 18-6: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (25°C)

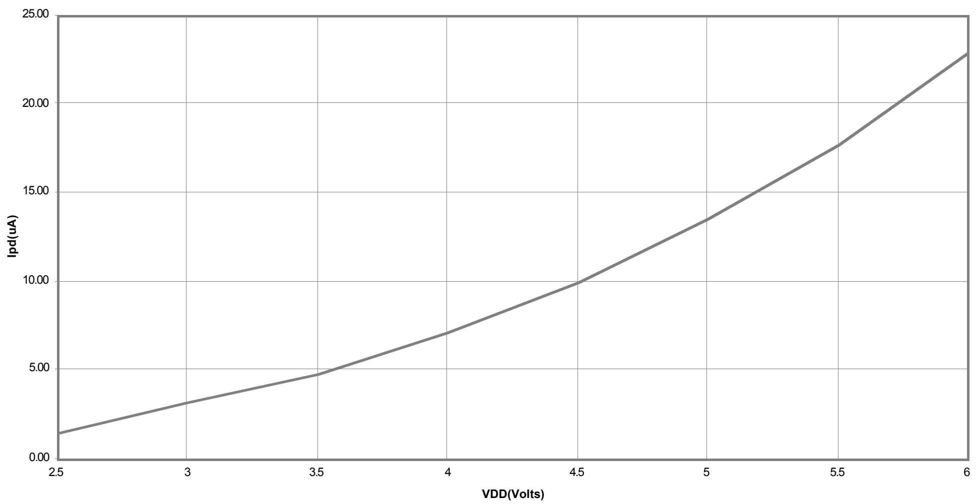


FIGURE 18-7: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs. VDD

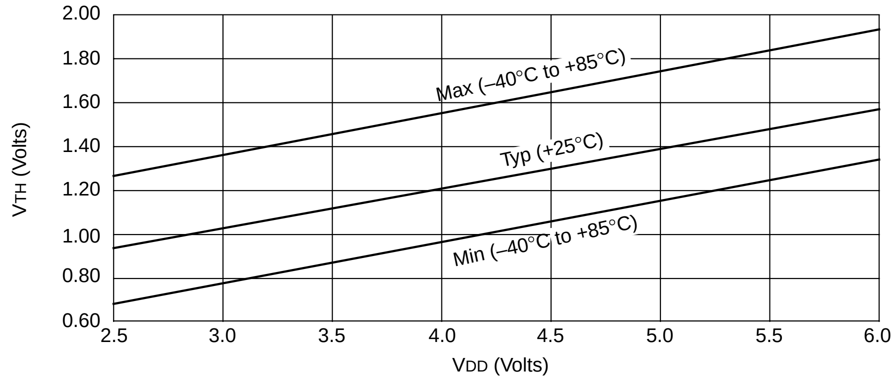
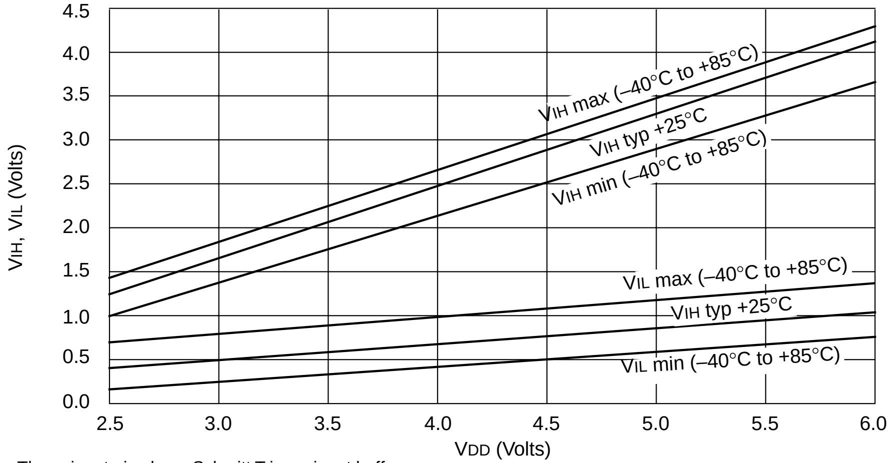


FIGURE 18-8: VIH, VIL OF $\overline{\text{MCLR}}$, T0CKI AND OSC1 (IN RC MODE) vs. VDD



Note: These input pins have Schmitt Trigger input buffers.

FIGURE 18-9: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs. VDD

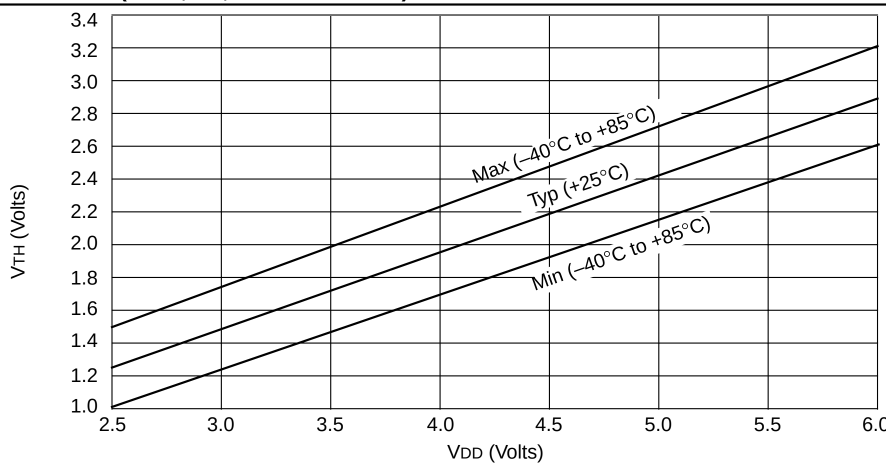


FIGURE 18-10: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 20 pF, 25°C)

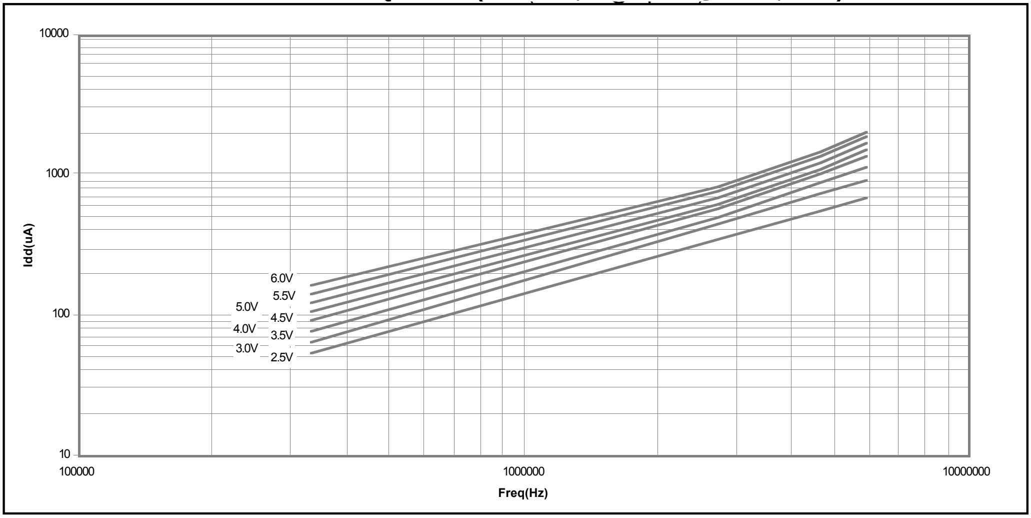


FIGURE 18-11: MAXIMUM IDD vs. FREQUENCY (WDT DIS, RC MODE @ 20 pF, –40°C TO +85°C)

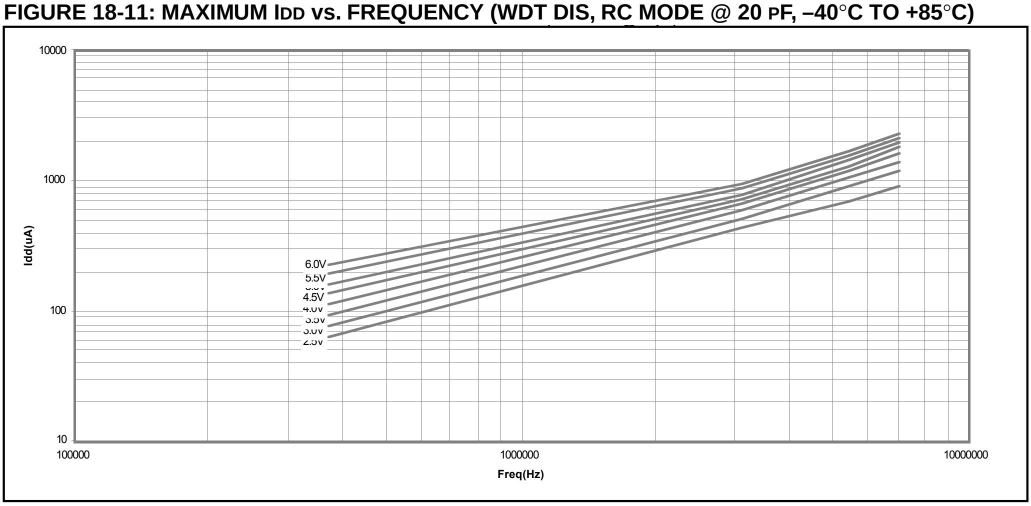


FIGURE 18-12: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 100 pF, 25°C)

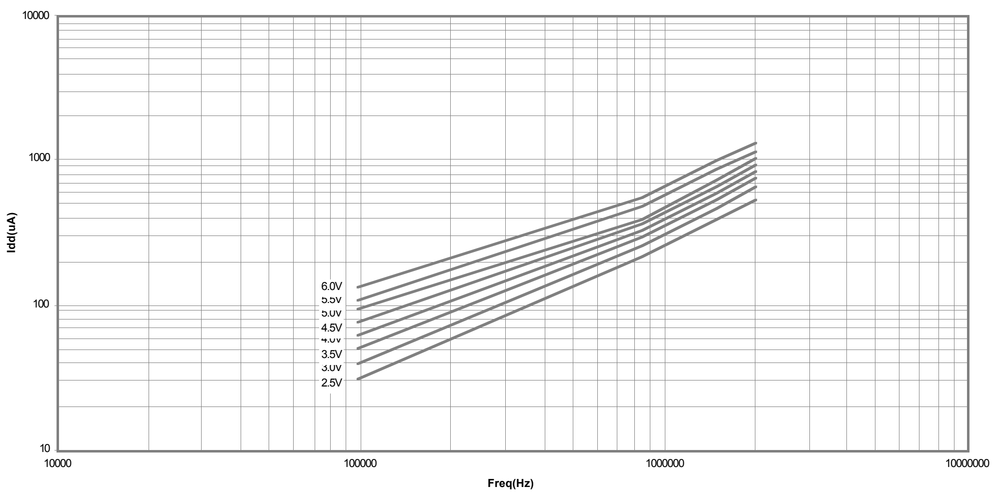


FIGURE 18-13: MAXIMUM IDD vs. FREQUENCY (WDT DIS, RC MODE @ 100 pF, –40°C TO +85°C)

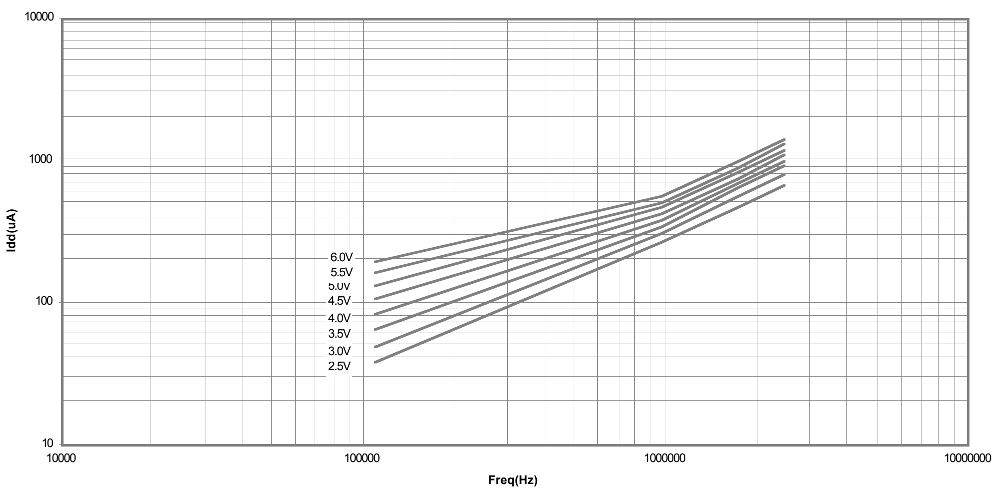


FIGURE 18-14: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 300 pF, 25°C)

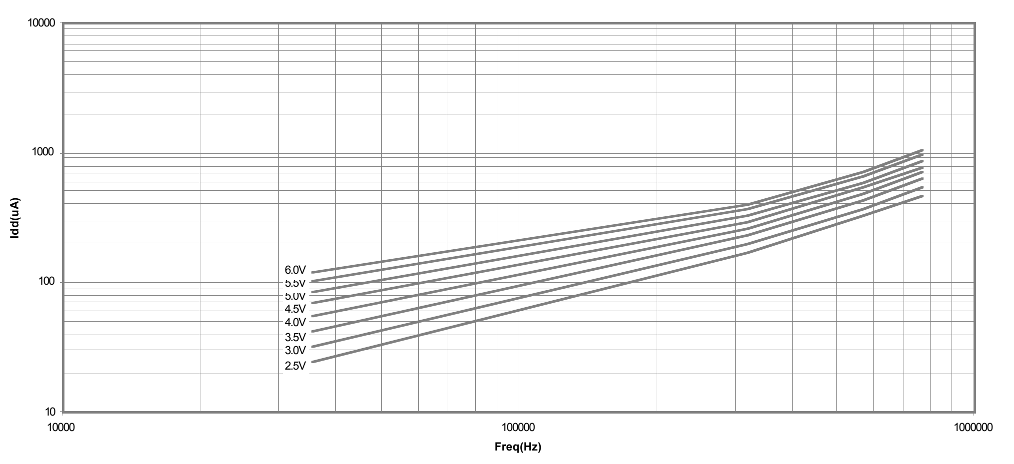


FIGURE 18-15: MAXIMUM IDD vs. FREQUENCY (WDT DIS, RC MODE @ 300 pF, –40°C TO +85°C)

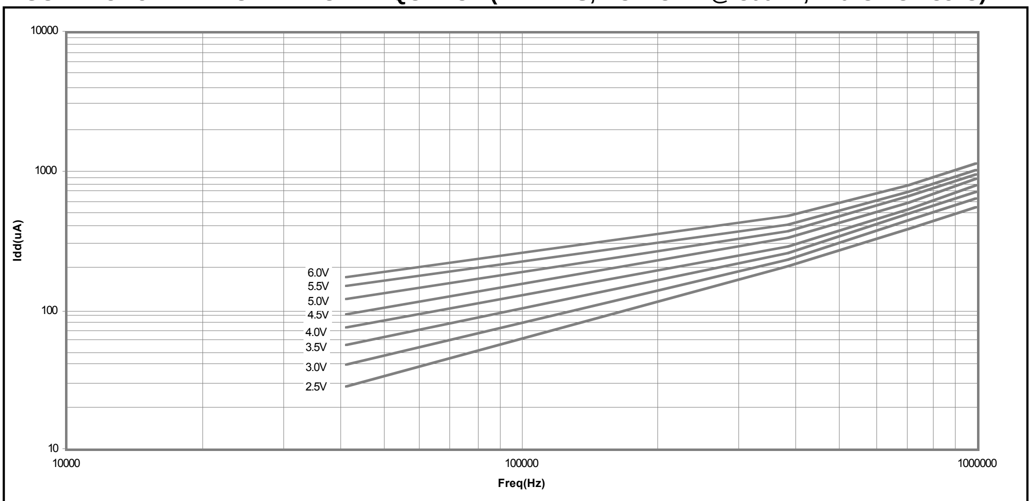


FIGURE 18-16: WDT TIMER TIME-OUT PERIOD vs. VDD

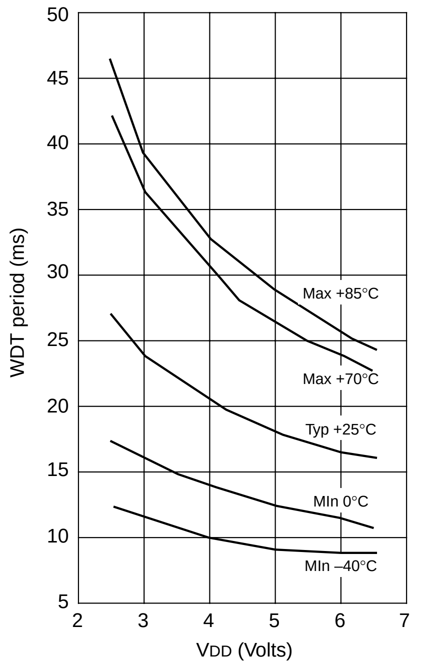


TABLE 18-2: INPUT CAPACITANCE FOR PIC16C54A/C58A

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{MCLR}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

FIGURE 18-17: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD

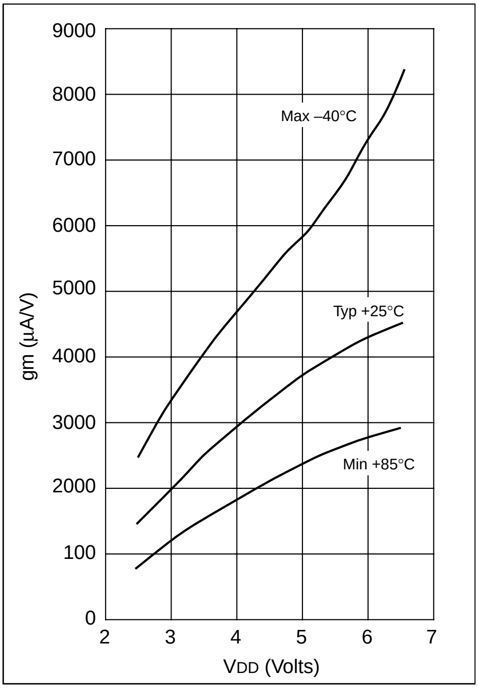


FIGURE 18-18: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

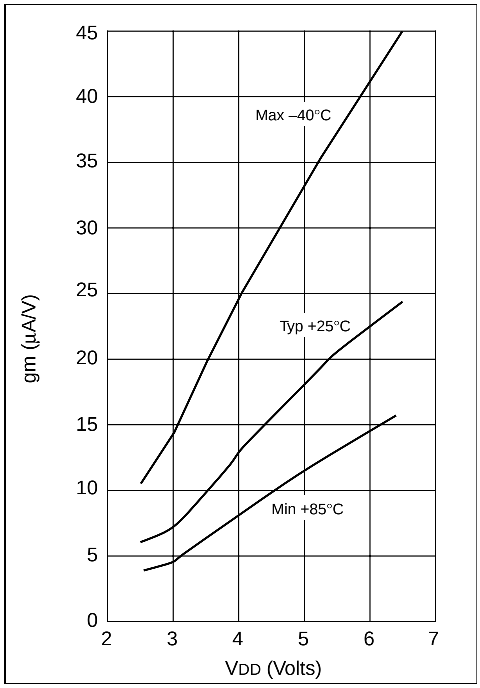


FIGURE 18-19: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD

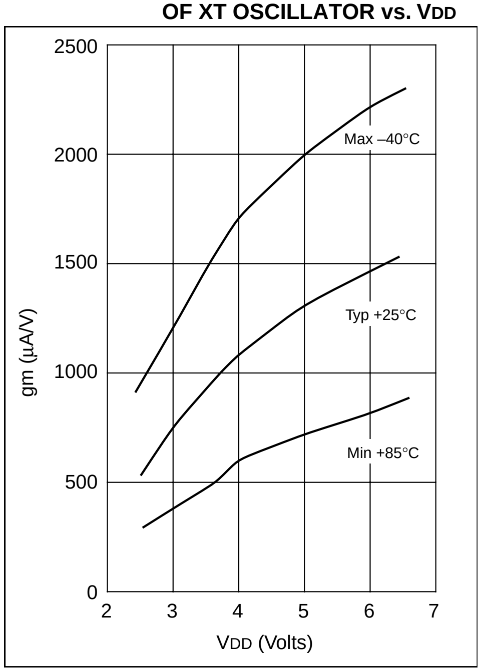


FIGURE 18-20: IOH vs. VOH, VDD = 3 V

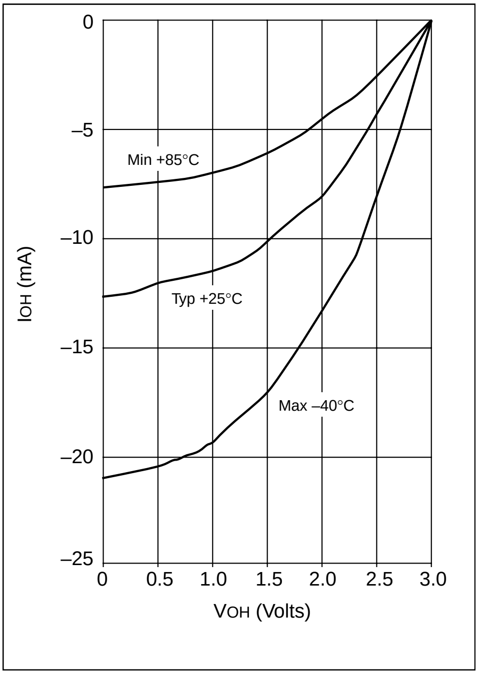


FIGURE 18-21: IOH vs. VOH, VDD = 5 V

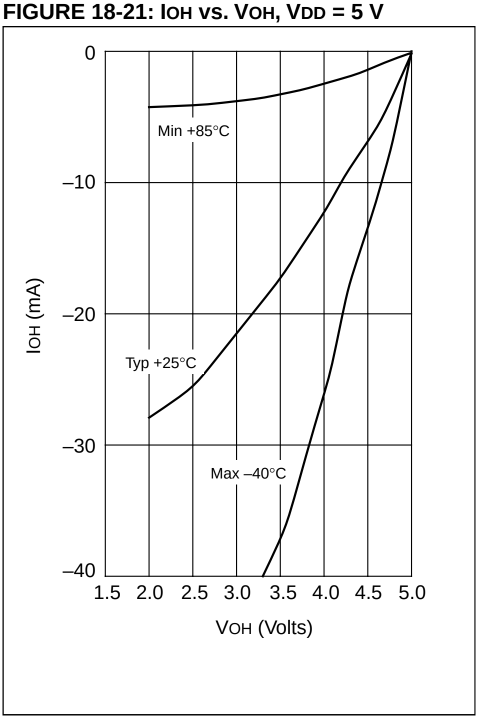


FIGURE 18-22: IOL vs. VOL, VDD = 3 V

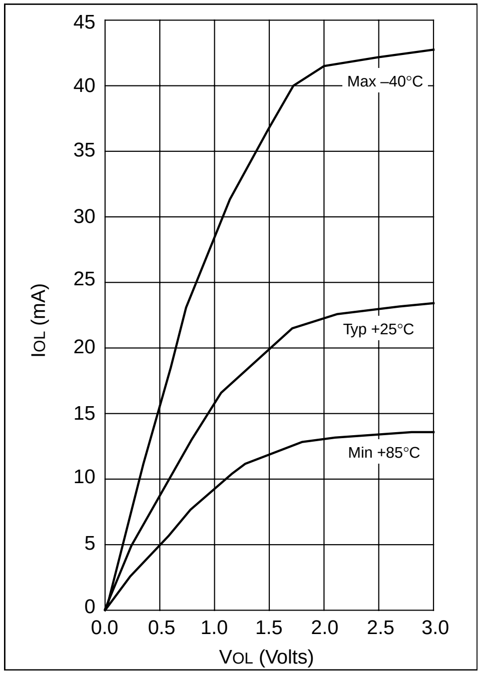
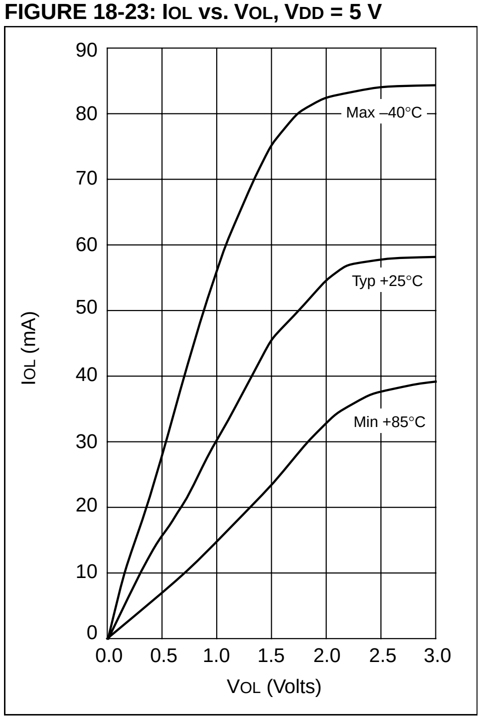


FIGURE 18-23: IOL vs. VOL, VDD = 5 V



NOTES:

19.0 ELECTRICAL CHARACTERISTICS - PIC16C54B/C54C/CR54B/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B

Absolute Maximum Ratings†

Ambient temperature under bias..–55°C to +125°C
Storage temperature .... –65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ....0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS}..0 to +14V
Voltage on all other pins with respect to V_{SS} .... –0.6V to (V_{DD} + 0.6V)
Total power dissipation(1) ....800 mW
Max. current out of V_{SS} pin...150 mA
Max. current into V_{DD} pin ....100 mA
Max. current into an input pin (T0CKI only)..±500 µA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})..±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ....±20 mA
Max. output current sunk by any I/O pin...25 mA
Max. output current sourced by any I/O pin ....20 mA
Max. output current sourced by a single I/O Port A ....50 mA
Max. output current sourced by a single I/O Port B ....50 mA
Max. output current sunk by a single I/OPort A..50 mA
Max. output current sunk by a single I/O Port B ....50 mA

Note 1: Power dissipation is calculated as follows: Pdis = V_{DD} x {I_{DD} - $\sum$ I_{OH}} + $\sum$ {(V_{DD}-V_{OH}) x I_{OH}} + $\sum$(V_{OL} x I_{OL})

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 19-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C5X-04	PIC16C5X-20	PIC16C5X/JW
RC	V_{DD}: 3.0V to 5.5V I_{DD}: 2.4 mA max. at 5.5V I_{PD}: 4.0 μA max. at 3.0V WDT dis Freq: 4 MHz max.	V_{DD}: 3.0V to 5.5V I_{DD}: 1.7 mA typ. at 5.5V I_{PD}: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	V_{DD}: 3.0V to 5.5V I_{DD}: 2.4 mA max. at 5.5V I_{PD}: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.
XT	V_{DD}: 3.0V to 5.5V I_{DD} 2.4 mA max. at 5.5V I_{PD}: 4.0 μA max. at 3.0V WDT dis Freq: 4 MHz max.	V_{DD}: 3.0V to 5.5V I_{DD}: 1.7 mA typ. at 5.5V I_{PD}: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	V_{DD}: 3.0V to 5.5V I_{DD} 2.4 mA max. at 5.5V I_{PD}: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.
HS	N/A	V_{DD}: 4.5V to 5.5V I_{DD}: 16 mA max. at 5.5V I_{PD}: 4.0 μA max. at 3.0V WDT dis Freq: 20 MHz max.	V_{DD}: 4.5V to 5.5V I_{DD}: 16 mA max. at 5.5V I_{PD}: 4.0 μA max. at 3.0V WDT dis Freq: 20 MHz max.
LP	V_{DD}: 3.0V to 5.5V I_{DD}: 14 μA typ. at 32kHz, 3.0V I_{PD}: 0.25 μA typ. at 3.0V WDT dis Freq: 200 kHz max.	N/A	V_{DD}: 3.0V to 5.5V I_{DD}: 32 μA max. at 32kHz, 3.0V WDT dis I_{PD}: 4.0 μA max. at 3.0V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

19.1 DC Characteristics: PIC16C54B/C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial) PIC16CR54B/CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial) PIC16C54B/C54C/C55A/C56A/C57C/C58B-04I, 20I (Industrial) PIC16CR54B/CR/54C/CR56A/CR57C/CR58B-04I, 20I (Industrial)

DC Characteristics Power Supply Pins	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ T_A ≤ +70°C (commercial) –40°C ≤ T_A ≤ +85°C (industrial)					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage XT, RC and LP options HS option	V_{DD}	 3.0 4.5	 — —	 5.5 5.5	 V V	
RAM Data Retention Voltage(2)	V_{DR}	—	1.5*	—	V	Device in SLEEP mode
V_{DD} start voltage to ensure Power-On Reset	V_{POR}	—	V_{SS}	—	V	See Section 7.4 for details on Power-on Reset
V_{DD} rise rate to ensure Power-On Reset	S_{VDD}	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) XT and RC(4) options HS option LP option, Commercial LP option, Industrial	I_{DD}	 — — — —	 1.8 4.5 14 17	 2.4 16 32 40	 mA mA μA μA	 F_{OSC} = 4.0 MHz, V_{DD} = 5.5V F_{OSC} = 20 MHz, V_{DD} = 5.5V F_{OSC} = 32 kHz, V_{DD} = 3.0V, WDT disabled F_{OSC} = 32 kHz, V_{DD} = 3.0V, WDT disabled
Power Down Current(5) Commercial Industrial 	I_{PD}	 — — — —	 4.0 0.25 4.0 0.25	 12 4.0 14 5.0	 μA μA μA μA	 V_{DD} = 3.0V, WDT enabled V_{DD} = 3.0V, WDT disabled V_{DD} = 3.0V, WDT enabled V_{DD} = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{SS}, T0CKI = V_{DD}, $\overline{MCLR}$ = V_{DD}; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2Rext$ (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} and V_{SS}.

19.2 DC Characteristics: PIC16C54B/C54C/C55A/C56A/C57C/C58B-04E, 20E (Extended) PIC16CR54B/CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)

DC Characteristics **Power Supply Pins**						**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (extended)
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage XT and RC options HS option	V_{DD}	 3.0 4.5	 — —	 5.5 5.5	 V V	
RAM Data Retention Voltage(2)	V_{DR}	—	1.5*	—	V	Device in SLEEP mode
V_{DD} start voltage to ensure Power-On Reset	V_{POR}	—	V_{SS}	—	V	See Section 7.4 for details on Power-on Reset
V_{DD} rise rate to ensure Power-On Reset	S_{VDD}	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) XT and RC(4) options HS option	I_{DD}	 — —	 1.8 9.0	 3.3 20	 mA mA	 F_{OSC} = 4.0 MHz, V_{DD} = 5.5V F_{OSC} = 20 MHz, V_{DD} = 5.5V
Power Down Current(5)	I_{PD}	— —	0.3 4.5	18 22	µA µA	V_{DD} = 3.5V, WDT disabled V_{DD} = 3.5V, WDT enabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
   a) The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{ss}, T0CKI = V_{DD}, $\overline{MCLR}$ = V_{DD}; WDT enabled/disabled as specified.
   b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: $I_R = V_{DD}/2Rext$ (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} and V_{SS}.

19.3 DC Characteristics: PIC16LC5X-04, PIC16LCR5X-04 (Commercial) PIC16LC5X-04I, PIC16LCR5X-04I (Industrial)

DC Characteristics Power Supply Pins						**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
XT and RC options		3.0	—	5.5	V	
LP options		2.5	—	5.5	V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
XT and RC(4) options		—	0.5	2.4	mA	FOSC = 4.0 MHz, VDD = 5.5V
LP option, Commercial		—	11	27	μA	FOSC = 32 kHz, VDD = 2.5V WDT disabled
LP option, Industrial		—	14	35	μA	FOSC = 32 kHz, VDD = 2.5V WDT disabled
Power Down Current(5)	IPD					
Commercial		—	2.5	10	μA	VDD = 2.5V, WDT enabled
		—	0.25	2.0	μA	VDD = 2.5V, WDT disabled
Industrial		—	2.5	12	μA	VDD = 2.5V, WDT enabled
		—	0.25	3.0	μA	VDD = 2.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

19.4 DC Characteristics: PIC16C54B/C54C/C55A/C56A/C57C/C58B-04, 20, PIC16LCR5X-04 (Commercial) PIC16CR54B/CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial) PIC16CR5X-04I, 20I (Commercial) PIC16C54B/C54C/C55A/C56A/C57C/C58B-04I, 20I, PIC16LC5X-04I (Industrial) PIC16C54B/C54C/C55A/C56A/C57C/C58B-04E, 20E (Extended)

DC Characteristics All Pins Except Power Supply Pins	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 19.1, Section 19.2 and Section 19.3.					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O Ports		Vss	—	0.8 VDD	V	4.5V <VDD ≤ 5.5V
I/O Ports		Vss	—	0.15 VDD	V	otherwise
$\overline{\text{MCLR}}$ (Schmitt Trigger)		Vss	—	0.15 VDD	V	
T0CKI (Schmitt Trigger)		Vss	—	0.15 VDD	V	
OSC1 (Schmitt Trigger)		Vss	—	0.15 VDD	V	RC option only(4)
OSC1				0.3 VDD	—	XT, HS and LP options
Input High Voltage	VIH					
		2.0	—	VDD	V	4.5V < VDD ≤ 5.5V(5)
I/O ports		0.25 VDD+0.8V	—	VDD	V	otherwise
$\overline{\text{MCLR}}$ (Schmitt Trigger)		0.85 VDD	—	VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD	—	VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD	—	VDD	V	RC option only(4)
OSC1		0.7 VDD	—	VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*	—	—	V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		-1.0	0.5	+1.0	μA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
$\overline{\text{MCLR}}$		-5.0	—	+5.0	μA	VPIN = VSS +0.25V(2)
			0.5	+3.0	μA	VPIN = VDD(2)
T0CKI		-3.0	0.5	+3.0	μA	VSS ≤ VPIN ≤ VDD
OSC1		-3.0	0.5	—	μA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports		—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage	VOH					
I/O ports(3)		VDD-0.7	—	—	V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD-0.7	—	—	V	IOH = -1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the $\overline{\text{MCLR}}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

19.5 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

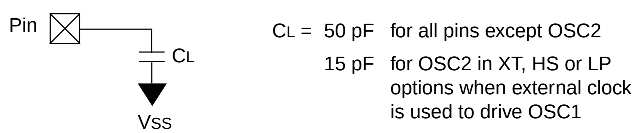
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 19-1: LOAD CONDITIONS - PIC16C54B/C54C/CR54B/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B, PIC16CR5X



19.6 Timing Diagrams and Specifications

FIGURE 19-2: EXTERNAL CLOCK TIMING - PIC16C5X, PIC16CR5X

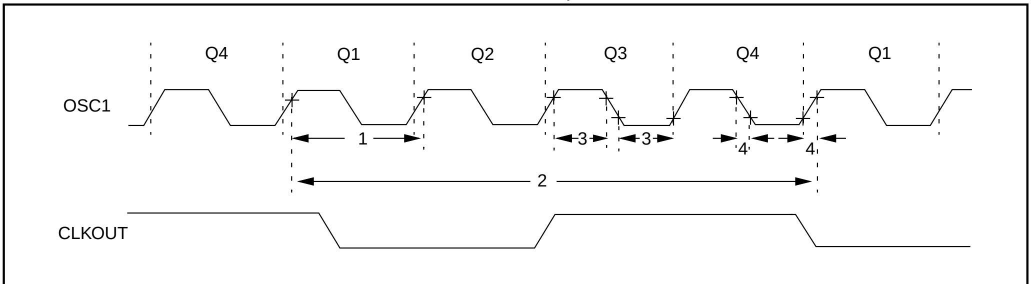


TABLE 19-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 19.1, Section 19.2 and Section 19.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	FOSC	External CLKIN Frequency(2)	DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4.0	MHz	RC osc mode
			0.455	—	4.0	MHz	XT osc mode
			4	—	4.0	MHz	HS osc mode (04)
			4	—	20	MHz	HS osc mode (20)
			5	—	200	kHz	LP osc mode
1	TOSC	External CLKIN Period(2)	250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	µs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	2,200	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	µs	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

TABLE 19-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X (CON'T)

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 19.1, Section 19.2 and Section 19.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

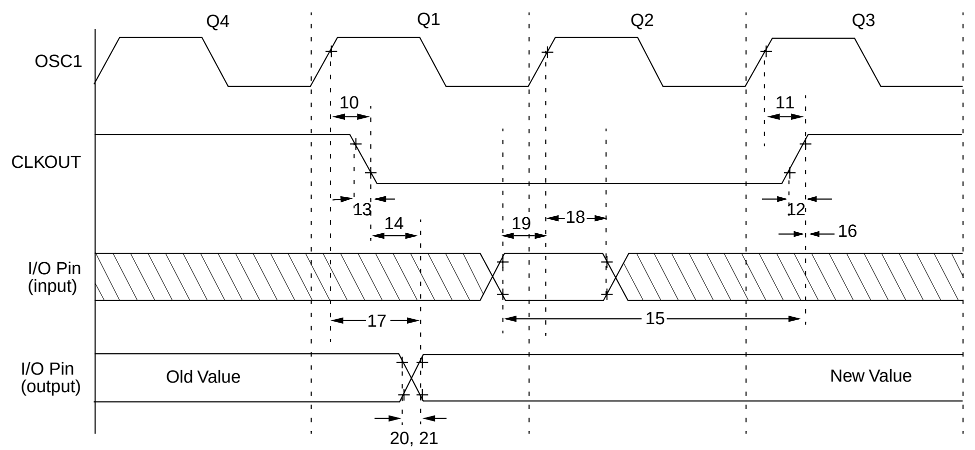
* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 19-3: CLKOUT AND I/O TIMING - PIC16C5X, PIC16CR5X



Note: Refer to Figure 19-1 for load conditions.

TABLE 19-3: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 19.1, Section 19.2 and Section 19.3.					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time(2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

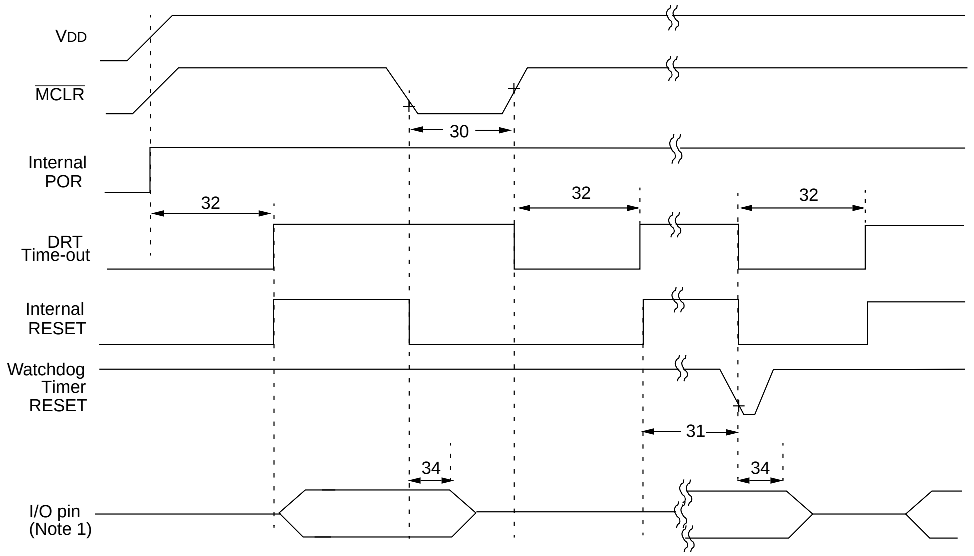
** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 19-1 for loading conditions.

FIGURE 19-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X, PIC16CR5X



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 19-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X, PIC16CR5X

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 19.1, Section 19.2 and Section 19.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	1000*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
34	Tioz	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low	100*	300*	1000*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-5: TIMER0 CLOCK TIMINGS - PIC16C5X, PIC16CR5X

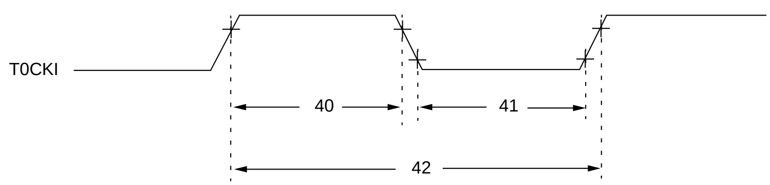


TABLE 19-5: TIMER0 CLOCK REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 19.1, Section 19.2 and Section 19.3.					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or (TCY + 40)* / N	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

20.0 DC AND AC CHARACTERISTICS - PIC16C54B/C54C/CR54B/CR54C/C55A/C56A/CR56A/C57C /CR57C/C58B/CR58B

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean – 3σ) respectively, where σ is standard deviation.

FIGURE 20-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

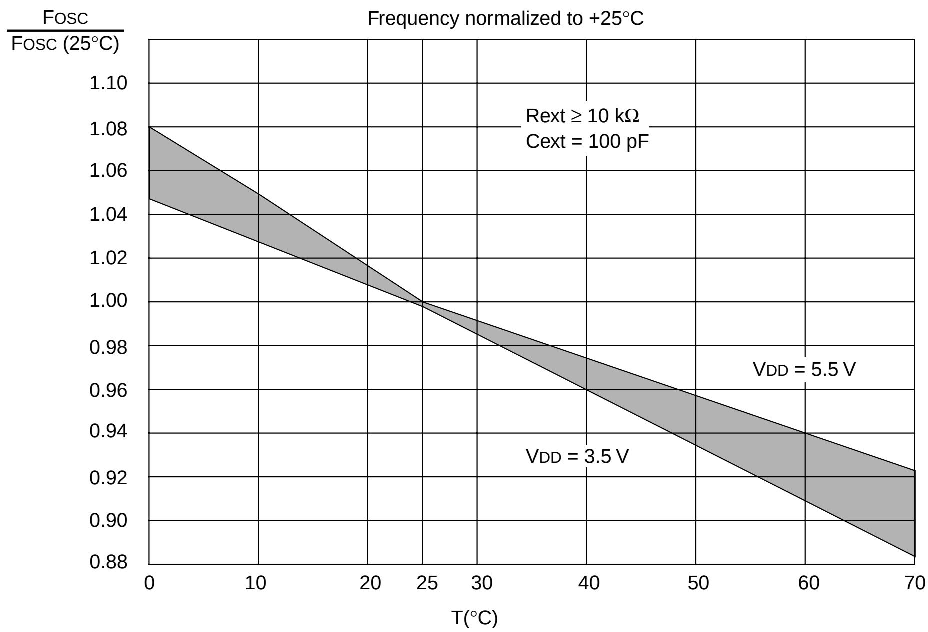


TABLE 20-1: RC OSCILLATOR FREQUENCIES

Cext	Rext	Average Fosc @ 5 V, 25°C	
20 pF	3.3 k	4.973 MHz	± 27%
	5 k	3.82 MHz	± 21%
	10 k	2.22 MHz	± 21%
	100 k	262.15 kHz	± 31%
100 pF	3.3 k	1.63 MHz	± 13%
	5 k	1.19 MHz	± 13%
	10 k	684.64 kHz	± 18%
	100 k	71.56 kHz	± 25%
300 pF	3.3 k	660 kHz	± 10%
	5.0 k	484.1 kHz	± 14%
	10 k	267.63 kHz	± 15%
	160 k	29.44 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for V_{DD} = 5 V.

FIGURE 20-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF

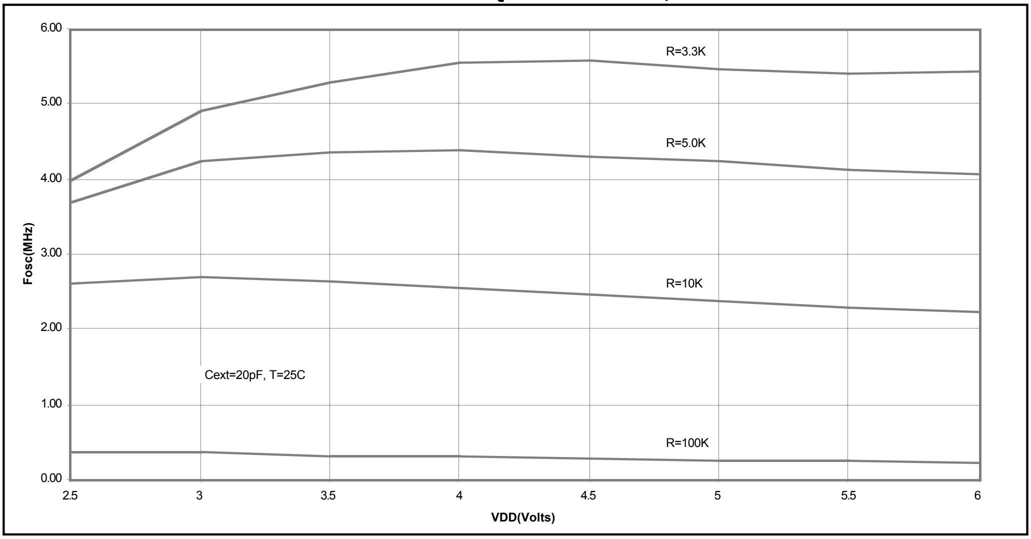


FIGURE 20-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF

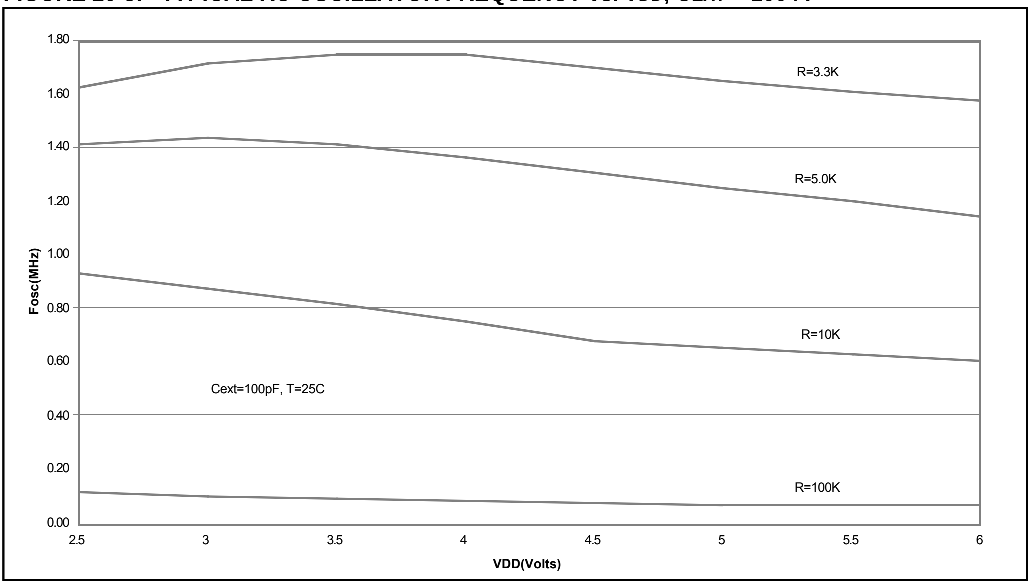


FIGURE 20-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF

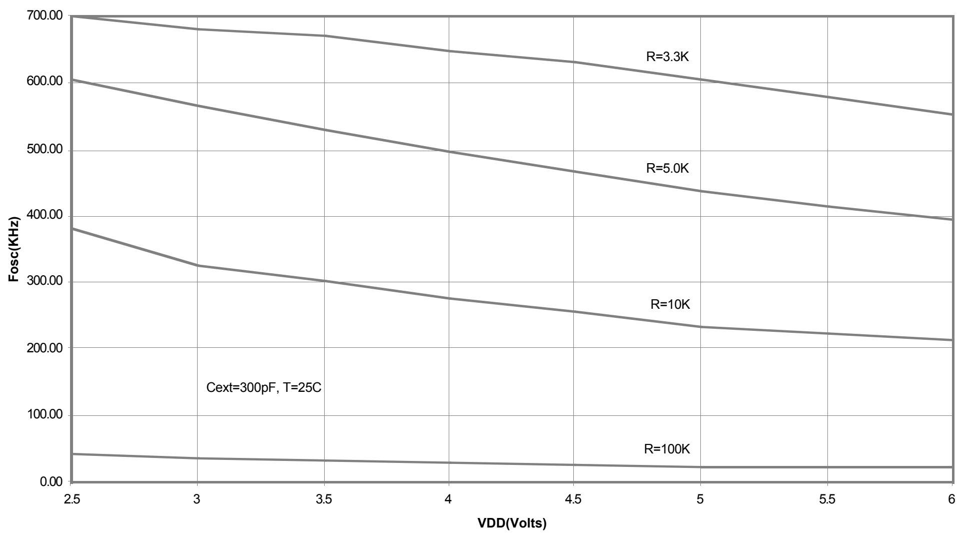


FIGURE 20-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)

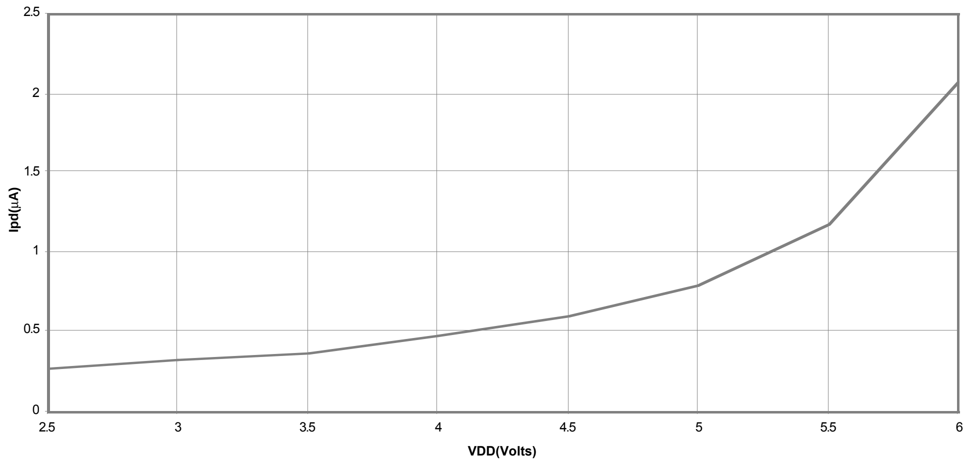


FIGURE 20-6: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (25°C)

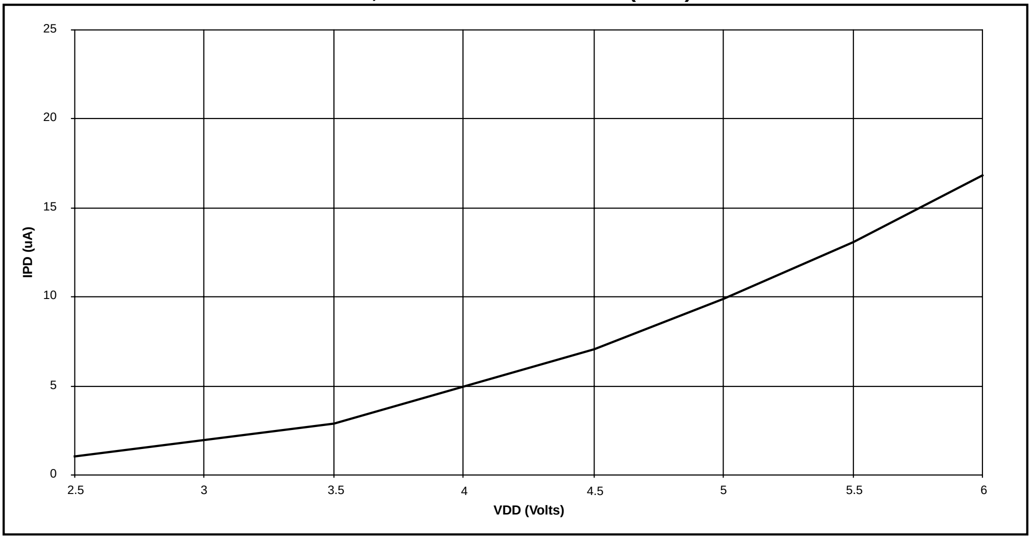


FIGURE 20-7: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (–40°C, 85°C)

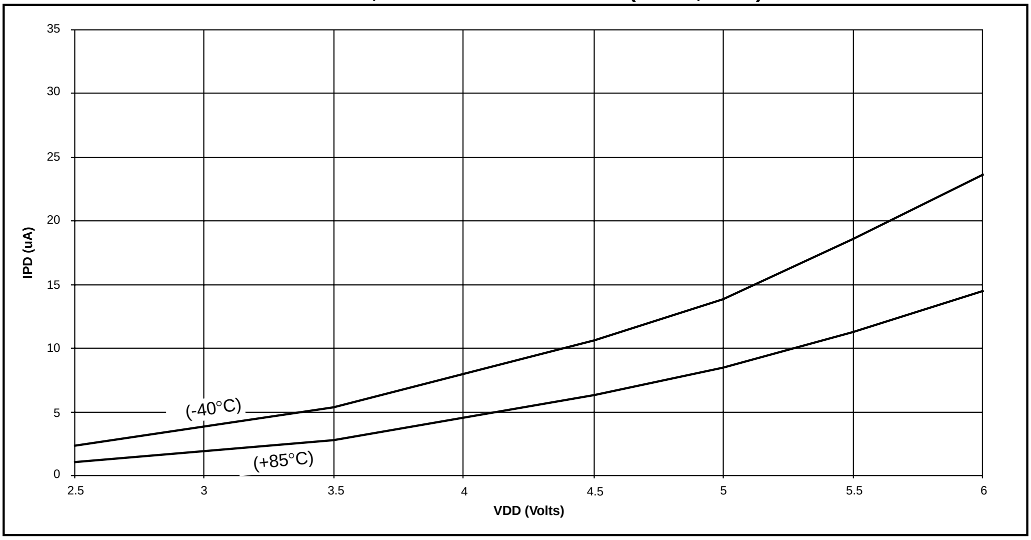


FIGURE 20-8: V_{TH} (INPUT THRESHOLD TRIP POINT VOLTAGE) OF I/O PINS vs. V_{DD}

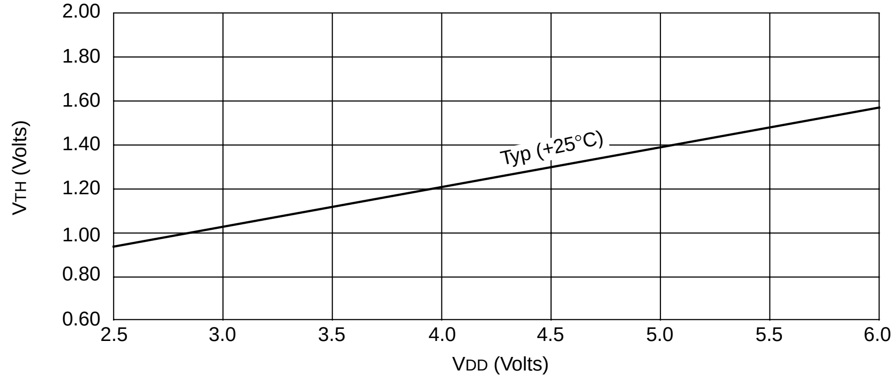
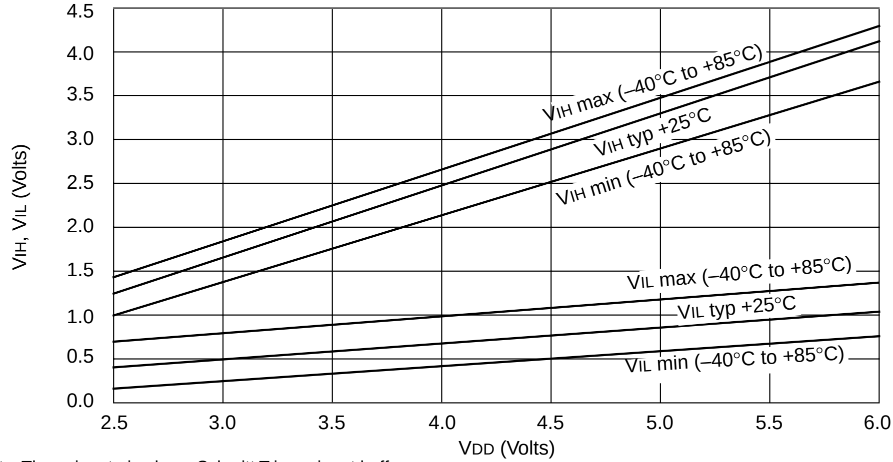


FIGURE 20-9: V_{IH}, V_{IL} OF $\overline{MCLR}$, T0CKI AND OSC1 (IN RC MODE) vs. V_{DD}



Note: These input pins have Schmitt Trigger input buffers.

FIGURE 20-10: V_{TH} (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs. V_{DD}

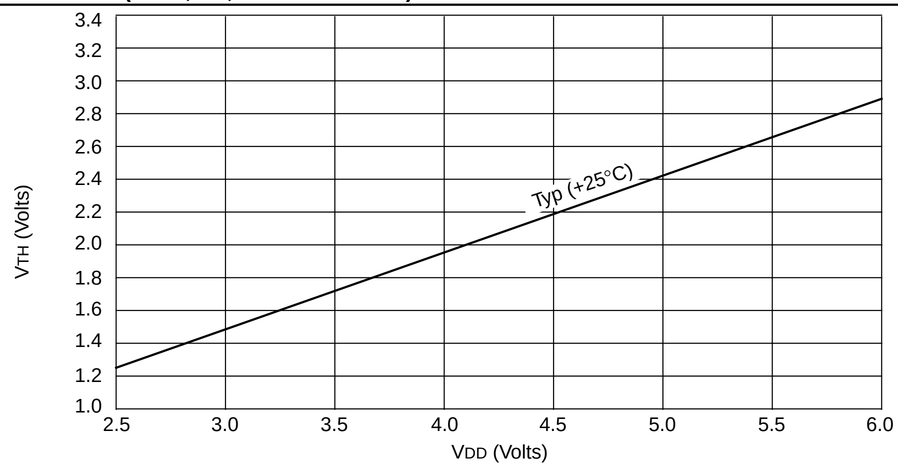


FIGURE 20-11: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 20 pF, 25°C)

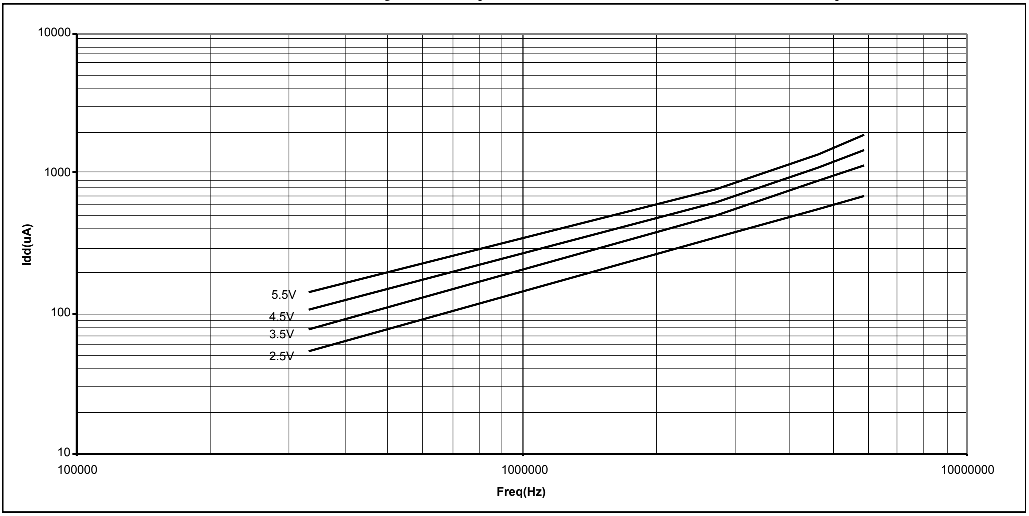


FIGURE 20-12: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 100 pF, 25°C)

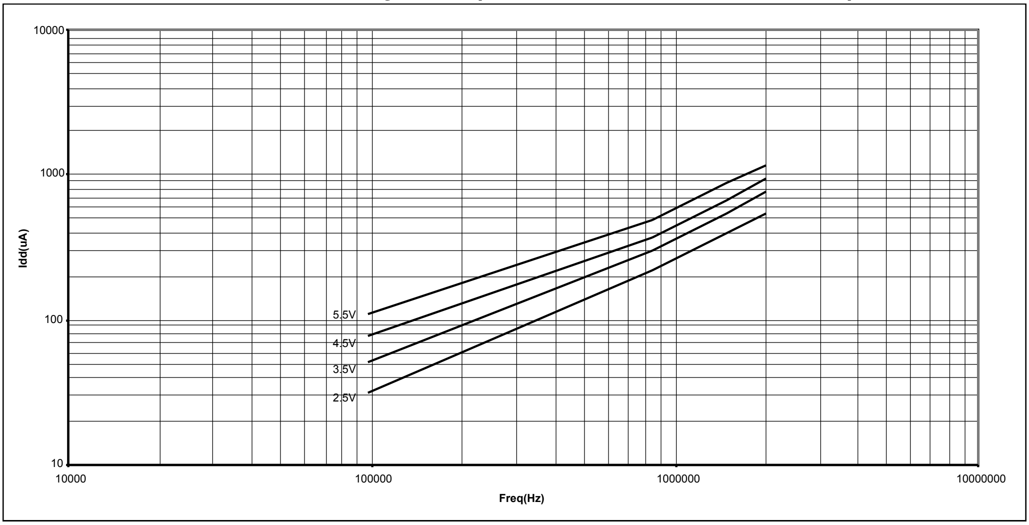


FIGURE 20-13: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 300 pF, 25°C)

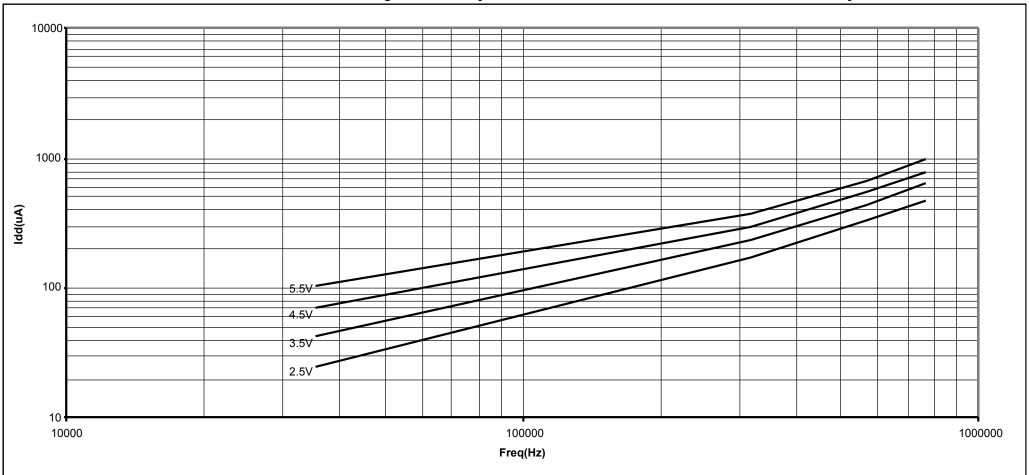


FIGURE 20-14: WDT TIMER TIME-OUT PERIOD vs. VDD

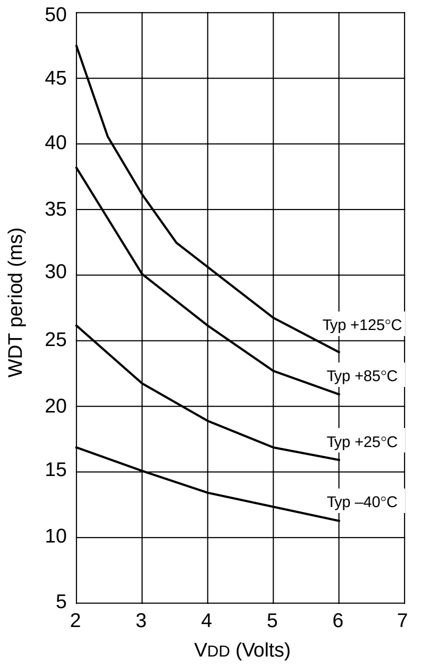


TABLE 20-2: INPUT CAPACITANCE FOR PIC16C54s/C56s/C58s

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{\text{MCLR}}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

FIGURE 20-15: IOH vs. VOH, VDD = 3 V

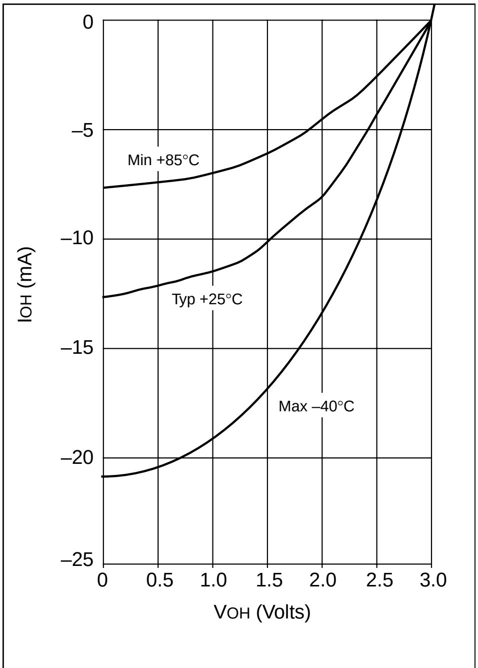


FIGURE 20-17: IOL vs. VOL, VDD = 3 V

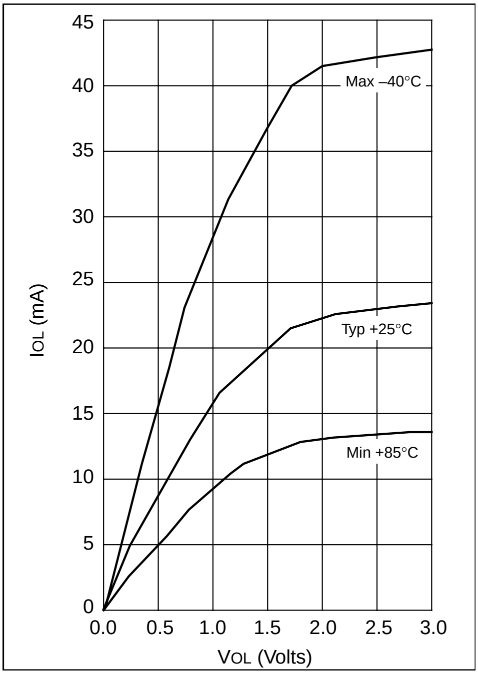


FIGURE 20-16: IOH vs. VOH, VDD = 5 V

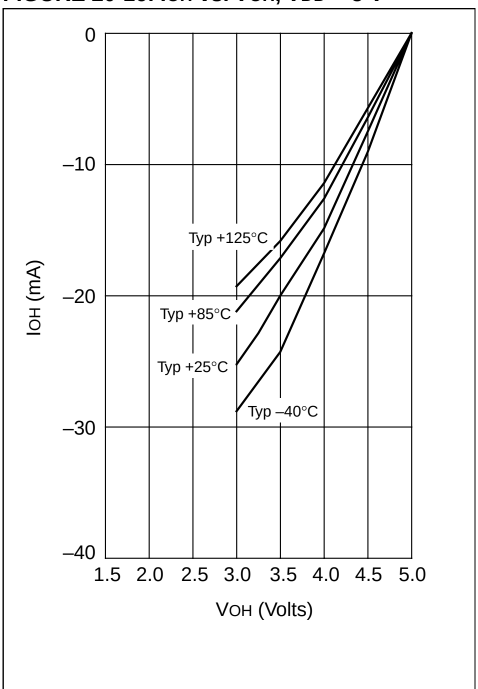
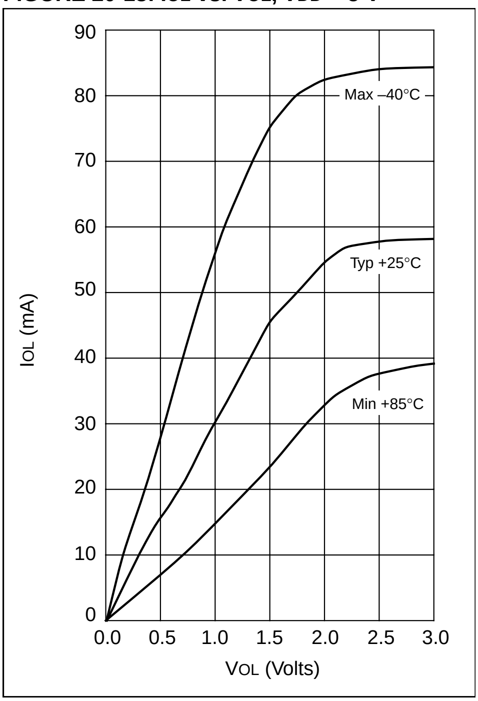


FIGURE 20-18: IOL vs. VOL, VDD = 5 V

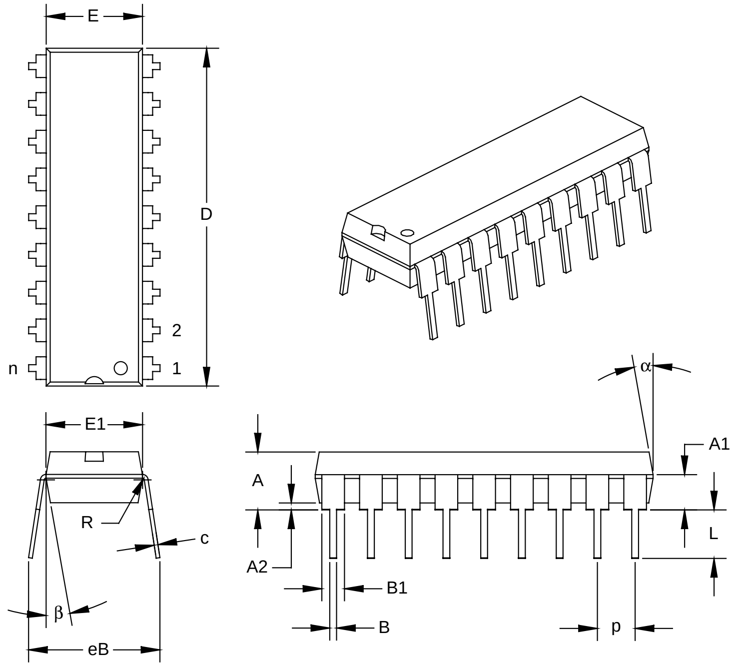


NOTES:

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21.0 PACKAGING INFORMATION

Package Type: K04-007 18-Lead Plastic Dual In-line (P) – 300 mil



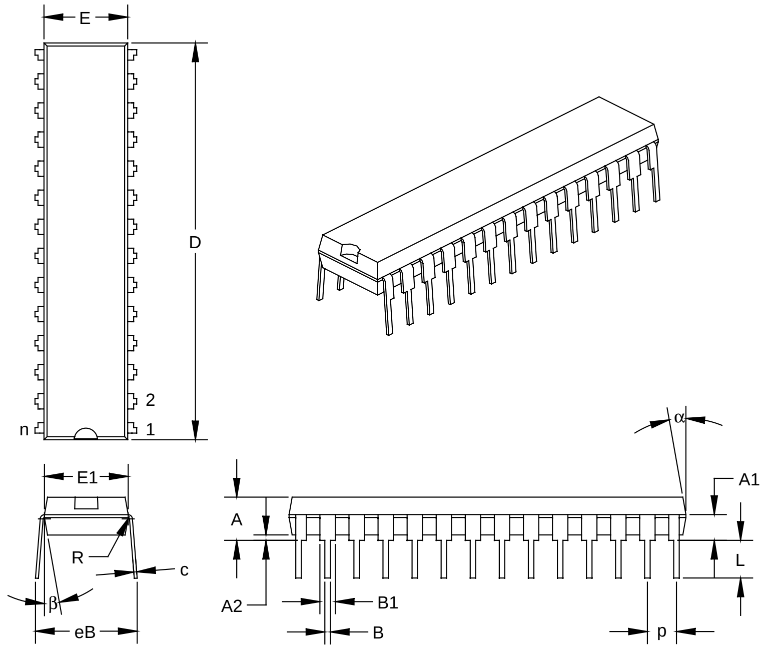
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		18			18	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.013	0.018	0.023	0.33	0.46	0.58
Upper Lead Width	B1†	0.055	0.060	0.065	1.40	1.52	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.005	0.010	0.015	0.13	0.25	0.38
Top to Seating Plane	A	0.110	0.155	0.155	2.79	3.94	3.94
Top of Lead to Seating Plane	A1	0.075	0.095	0.115	1.91	2.41	2.92
Base to Seating Plane	A2	0.000	0.020	0.020	0.00	0.51	0.51
Tip to Seating Plane	L	0.125	0.130	0.135	3.18	3.30	3.43
Package Length	D‡	0.890	0.895	0.900	22.61	22.73	22.86
Molded Package Width	E‡	0.245	0.255	0.265	6.22	6.48	6.73
Radius to Radius Width	E1	0.230	0.250	0.270	5.84	6.35	6.86
Overall Row Spacing	eB	0.310	0.349	0.387	7.87	8.85	9.83
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

† Dimension “B1” does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003” (0.076 mm) per side or 0.006” (0.152 mm) more than dimension “B1.”

‡ Dimensions “D” and “E” do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010” (0.254 mm) per side or 0.020” (0.508 mm) more than dimensions “D” or “E.”

Package Type: K04-070 28-Lead Skinny Plastic Dual In-line (SP) – 300 mil



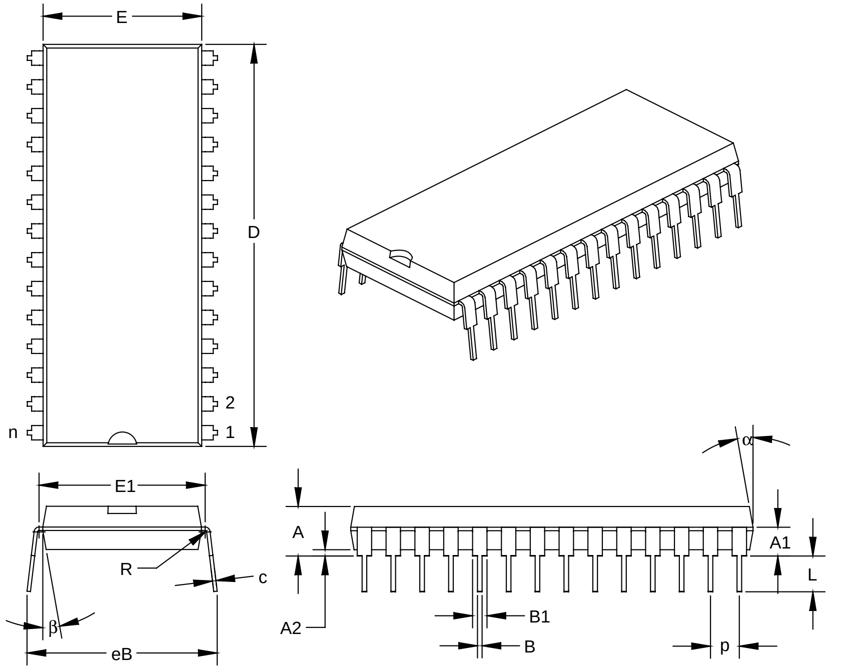
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		28			28	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.016	0.019	0.022	0.41	0.48	0.56
Upper Lead Width	B1†	0.040	0.053	0.065	1.02	1.33	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.140	0.150	0.160	3.56	3.81	4.06
Top of Lead to Seating Plane	A1	0.070	0.090	0.110	1.78	2.29	2.79
Base to Seating Plane	A2	0.015	0.020	0.025	0.38	0.51	0.64
Tip to Seating Plane	L	0.125	0.130	0.135	3.18	3.30	3.43
Package Length	D‡	1.345	1.365	1.385	34.16	34.67	35.18
Molded Package Width	E‡	0.280	0.288	0.295	7.11	7.30	7.49
Radius to Radius Width	E1	0.270	0.283	0.295	6.86	7.18	7.49
Overall Row Spacing	eB	0.320	0.350	0.380	8.13	8.89	9.65
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

† Dimension “B1” does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003” (0.076 mm) per side or 0.006” (0.152 mm) more than dimension “B1.”

‡ Dimensions “D” and “E” do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010” (0.254 mm) per side or 0.020” (0.508 mm) more than dimensions “D” or “E.”

Package Type: K04-079 28-Lead Plastic Dual In-line (P) – 600 mil



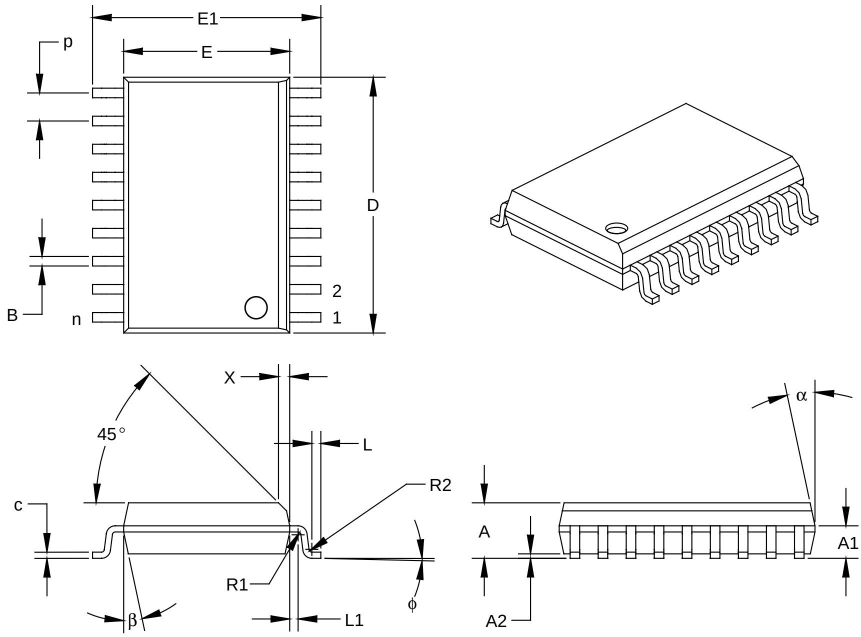
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.600			15.24	
Number of Pins	n		28			28	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.014	0.016	0.018	0.36	0.41	0.46
Upper Lead Width	B1†	0.040	0.050	0.060	1.02	1.27	1.52
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.012	0.015	0.20	0.29	0.38
Top to Seating Plane	A	0.160	0.173	0.185	4.06	4.38	4.70
Top of Lead to Seating Plane	A1	0.081	0.101	0.121	2.04	2.55	3.06
Base to Seating Plane	A2	0.015	0.023	0.030	0.38	0.57	0.76
Tip to Seating Plane	L	0.115	0.125	0.135	2.92	3.18	3.43
Package Length	D‡	1.380	1.395	1.465	35.05	35.43	37.20
Molded Package Width	E‡	0.505	0.550	0.555	12.80	13.97	14.10
Radius to Radius Width	E1	0.567	0.577	0.587	14.40	14.66	14.91
Overall Row Spacing	eB	0.640	0.660	0.680	16.26	16.76	17.27
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter.

† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

Package Type: K04-051 18-Lead Plastic Small Outline (SO) – Wide, 300 mil



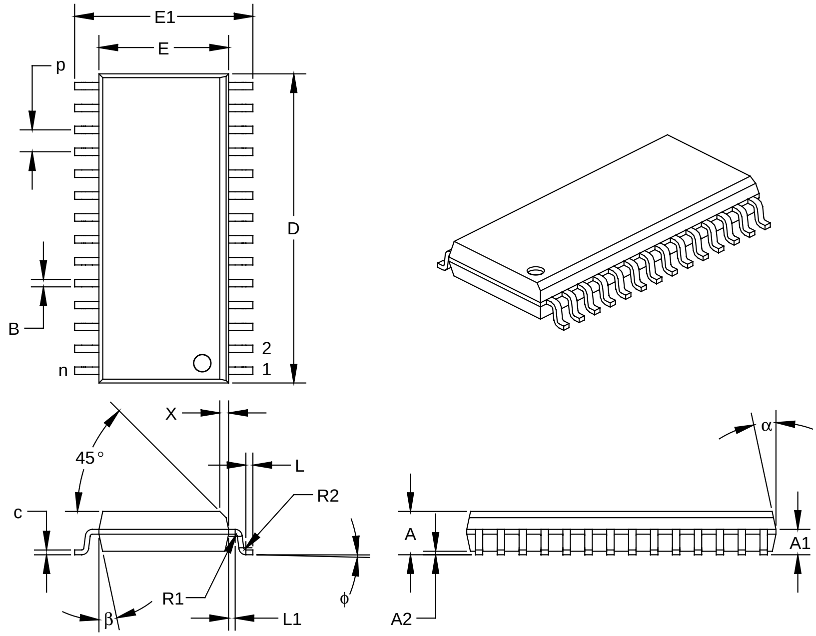
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		18			18	
Overall Pack. Height	A	0.093	0.099	0.104	2.36	2.50	2.64
Shoulder Height	A1	0.048	0.058	0.068	1.22	1.47	1.73
Standoff	A2	0.004	0.008	0.011	0.10	0.19	0.28
Molded Package Length	D‡	0.450	0.456	0.462	11.43	11.58	11.73
Molded Package Width	E‡	0.292	0.296	0.299	7.42	7.51	7.59
Outside Dimension	E1	0.394	0.407	0.419	10.01	10.33	10.64
Chamfer Distance	X	0.010	0.020	0.029	0.25	0.50	0.74
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
Lead Thickness	c	0.009	0.011	0.012	0.23	0.27	0.30
Lower Lead Width	B†	0.014	0.017	0.019	0.36	0.42	0.48
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter.

† Dimension “B” does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003” (0.076 mm) per side or 0.006” (0.152 mm) more than dimension “B.”

‡ Dimensions “D” and “E” do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010” (0.254 mm) per side or 0.020” (0.508 mm) more than dimensions “D” or “E.”

Package Type: K04-052 28-Lead Plastic Small Outline (SO) – Wide, 300 mil



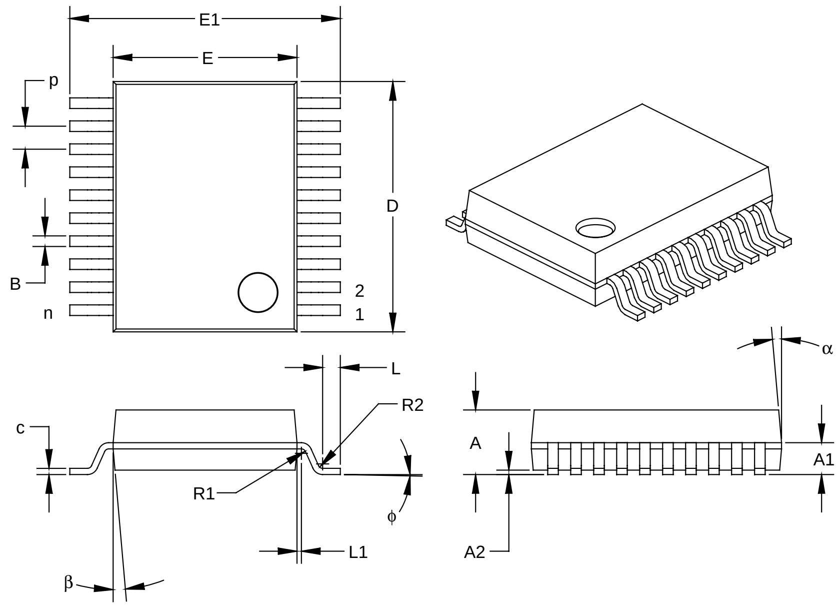
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		28			28	
Overall Pack. Height	A	0.093	0.099	0.104	2.36	2.50	2.64
Shoulder Height	A1	0.048	0.058	0.068	1.22	1.47	1.73
Standoff	A2	0.004	0.008	0.011	0.10	0.19	0.28
Molded Package Length	D‡	0.700	0.706	0.712	17.78	17.93	18.08
Molded Package Width	E‡	0.292	0.296	0.299	7.42	7.51	7.59
Outside Dimension	E1	0.394	0.407	0.419	10.01	10.33	10.64
Chamfer Distance	X	0.010	0.020	0.029	0.25	0.50	0.74
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
Lead Thickness	c	0.009	0.011	0.012	0.23	0.27	0.30
Lower Lead Width	B†	0.014	0.017	0.019	0.36	0.42	0.48
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter.

† Dimension “B” does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003” (0.076 mm) per side or 0.006” (0.152 mm) more than dimension “B.”

‡ Dimensions “D” and “E” do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010” (0.254 mm) per side or 0.020” (0.508 mm) more than dimensions “D” or “E.”

Package Type: K04-072 20-Lead Plastic Shrink Small Outine (SS) – 5.30 mm



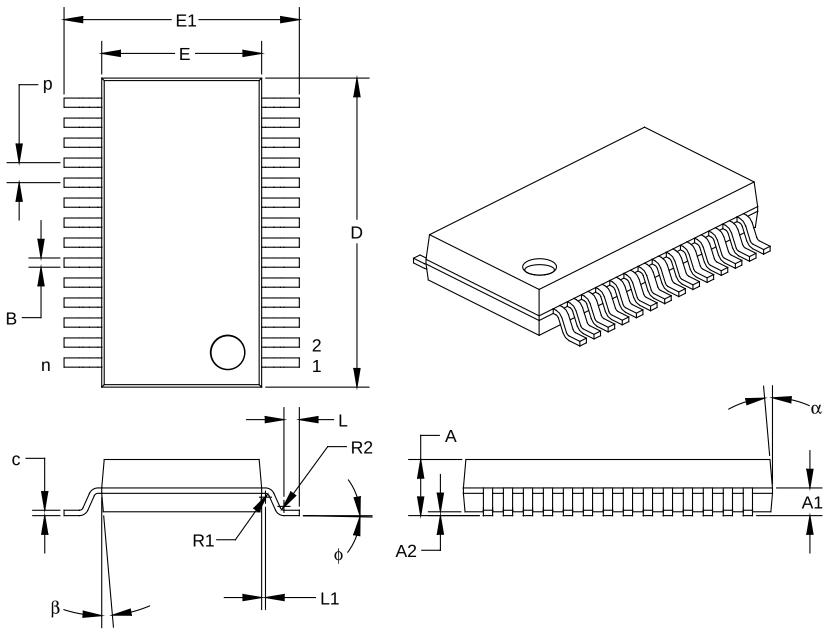
Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.026			0.65	
Number of Pins	n		20			20	
Overall Pack. Height	A	0.068	0.073	0.078	1.73	1.86	1.99
Shoulder Height	A1	0.026	0.036	0.046	0.66	0.91	1.17
Standoff	A2	0.002	0.005	0.008	0.05	0.13	0.21
Molded Package Length	D[‡]	0.278	0.283	0.289	7.07	7.20	7.33
Molded Package Width	E[‡]	0.205	0.208	0.212	5.20	5.29	5.38
Outside Dimension	E1	0.301	0.306	0.311	7.65	7.78	7.90
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.015	0.020	0.025	0.38	0.51	0.64
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.005	0.007	0.009	0.13	0.18	0.22
Lower Lead Width	B[†]	0.010	0.012	0.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

† Dimension “B” does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003” (0.076 mm) per side or 0.006” (0.152 mm) more than dimension “B.”

‡ Dimensions “D” and “E” do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010” (0.254 mm) per side or 0.020” (0.508 mm) more than dimensions “D” or “E.”

Package Type: K04-073 28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm



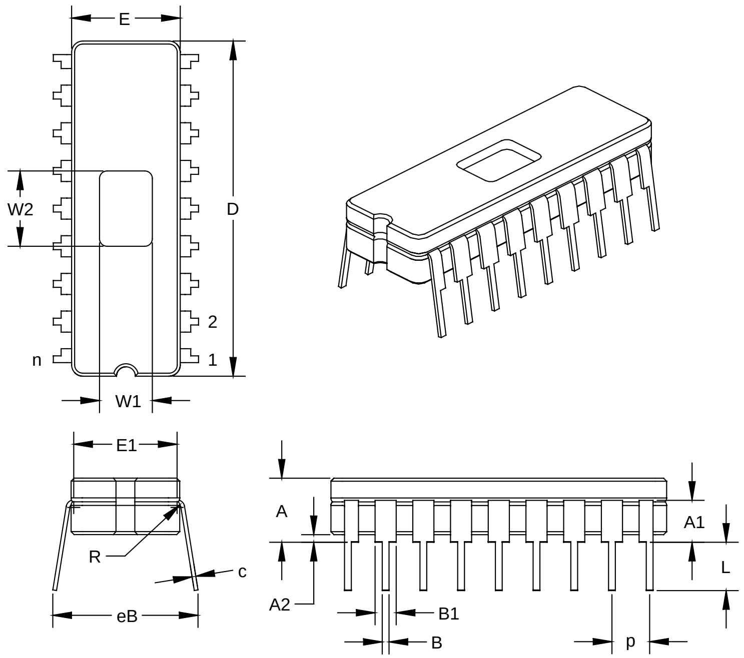
Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.026			0.65	
Number of Pins	n		28			28	
Overall Pack. Height	A	0.068	0.073	0.078	1.73	1.86	1.99
Shoulder Height	A1	0.026	0.036	0.046	0.66	0.91	1.17
Standoff	A2	0.002	0.005	0.008	0.05	0.13	0.21
Molded Package Length	D‡	0.396	0.402	0.407	10.07	10.20	10.33
Molded Package Width	E‡	0.205	0.208	0.212	5.20	5.29	5.38
Outside Dimension	E1	0.301	0.306	0.311	7.65	7.78	7.90
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.015	0.020	0.025	0.38	0.51	0.64
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.005	0.007	0.009	0.13	0.18	0.22
Lower Lead Width	B†	0.010	0.012	0.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter.

† Dimension “B” does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003” (0.076 mm) per side or 0.006” (0.152 mm) more than dimension “B.”

‡ Dimensions “D” and “E” do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010” (0.254 mm) per side or 0.020” (0.508 mm) more than dimensions “D” or “E.”

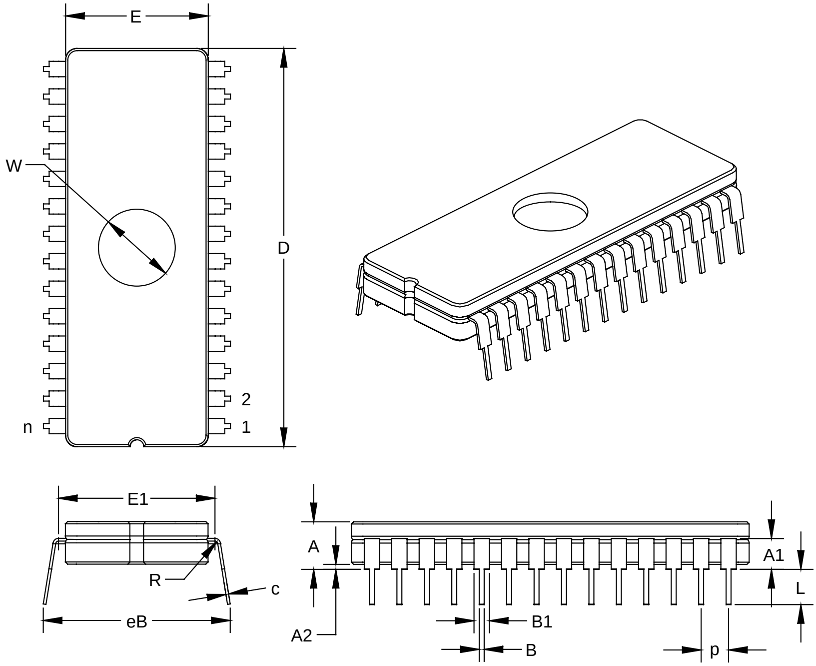
Package Type: K04-010 18-Lead Ceramic Dual In-line with Window (JW) – 300 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.300			7.62	
Number of Pins	n		18			18	
Pitch	p	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	B	0.016	0.019	0.021	0.41	0.47	0.53
Upper Lead Width	B1	0.050	0.055	0.060	1.27	1.40	1.52
Shoulder Radius	R	0.010	0.013	0.015	0.25	0.32	0.38
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.175	0.183	0.190	4.45	4.64	4.83
Top of Lead to Seating Plane	A1	0.091	0.111	0.131	2.31	2.82	3.33
Base to Seating Plane	A2	0.015	0.023	0.030	0.00	0.57	0.76
Tip to Seating Plane	L	0.125	0.138	0.150	3.18	3.49	3.81
Package Length	D	0.880	0.900	0.920	22.35	22.86	23.37
Package Width	E	0.285	0.298	0.310	7.24	7.56	7.87
Radius to Radius Width	E1	0.255	0.270	0.285	6.48	6.86	7.24
Overall Row Spacing	eB	0.345	0.385	0.425	8.76	9.78	10.80
Window Width	W1	0.130	0.140	0.150	0.13	0.14	0.15
Window Length	W2	0.190	0.200	0.210	0.19	0.2	0.21

* Controlling Parameter.

Package Type: K04-013 28-Lead Ceramic Dual In-line with Window (JW) – 600 mil



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
PCB Row Spacing			0.600			15.24	
Number of Pins	n		28			28	
Pitch	p	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	B	0.016	0.019	0.021	0.41	0.47	0.53
Upper Lead Width	B1	0.050	0.058	0.065	1.27	1.46	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.170	0.185	0.200	4.32	4.70	5.08
Top of Lead to Seating Plane	A1	0.110	0.128	0.146	2.78	3.24	3.70
Base to Seating Plane	A2	0.015	0.038	0.060	0.00	0.95	1.52
Tip to Seating Plane	L	0.125	0.138	0.150	3.18	3.49	3.81
Package Length	D	1.430	1.460	1.490	36.32	37.08	37.85
Package Width	E	0.514	0.520	0.526	13.06	13.21	13.36
Radius to Radius Width	E1	0.560	0.580	0.600	14.22	14.73	15.24
Overall Row Spacing	eB	0.610	0.660	0.710	15.49	16.76	18.03
Window Diameter	W	0.270	0.280	0.290	6.86	7.11	7.37

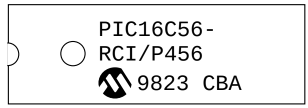
* Controlling Parameter.

21.1 Package Marking Information

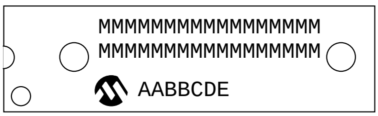
18-Lead PDIP



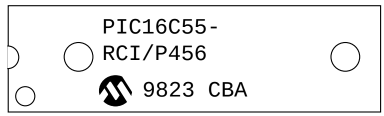
Example



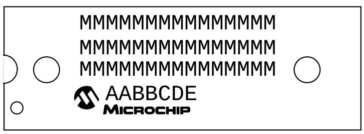
28-Lead Skinny PDIP (.300")



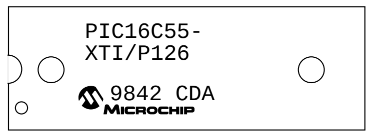
Example



28-Lead PDIP (.600")



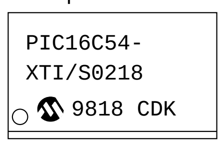
Example



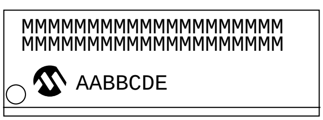
18-Lead SOIC



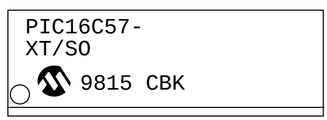
Example



28-Lead SOIC



Example



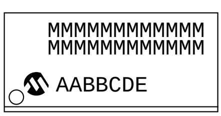
20-Lead SSOP



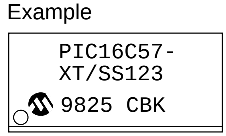
Example



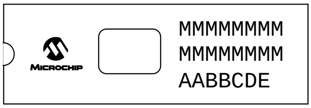
28-Lead SSOP



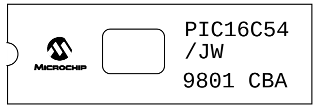
Example



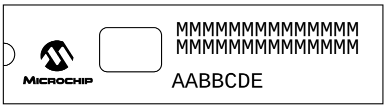
18-Lead CERDIP Windowed



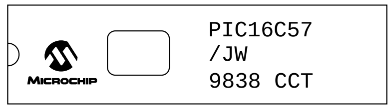
Example



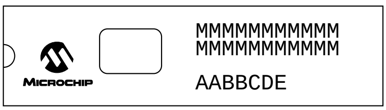
28-Lead CERDIP Skinny Windowed



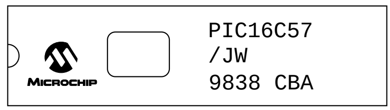
Example



28-Lead CERDIP Windowed



Example



Legend:		
	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week ‘01’)
	C	Facility code of the plant at which wafer is manufactured O = Outside Vendor C = 5” Line S = 6” Line H = 8” Line
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

NOTES:

APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

1. Check any `CALL`, `GOTO` or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to proper value for processor used.
6. Remove any use of the `ADDLW` and `SUBLW` instructions.
7. Rewrite any code segments that use interrupts.

NOTES:

INDEX

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web (WWW) site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape or Microsoft Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available by using your favorite Internet browser to attach to:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

ftp://ftp.futureone.com/pub/microchip

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

Systems Information and Upgrade Hot Line

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive any currently available upgrade kits.The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-602-786-7302 for the rest of the world.

980106

READER RESPONSE

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Application (optional):

Would you like a reply? ___Y ___N

Device: **PIC16C5X**   Literature Number: **DS30453B**

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this data sheet easy to follow? If not, why?

4. What additions to the data sheet do you think would enhance the structure and subject?

5. What deletions from the data sheet could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

8. How would you improve our software, systems, and silicon products?

PIC16C5X PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XX	X	/XX	XXX
Device	Frequency Range	Temperature Range	Package	Pattern

Device	PIC16C5X(2), PIC16C5XT(3) PIC16LC5X(2), PIC16LC5XT(3) PIC16CR5X(2), PIC16CR5XT(3) PIC16LCR5X(2), PIC16LCR5XT(3) PIC16LV5X(2), PIC16LV5XT(3)	
Frequency Range	02 04 10 20 b(1)	= 2 MHz = 4 MHz = 10 MHz = 20 MHz = No type for JW(4) devices
Temperature Range	b(1) I E	= 0°C to +70°C (Commercial) = -40°C to +85°C (Industrial) = -40°C to +125°C (Automotive)
Package	JW P SO SP SS	= Windowed CERDIP = PDIP = SOIC (Gull Wing, 300 mil body) = Skinny PDIP (28-pin, 300 mil body) = SSOP (209 mil body)
Pattern	3-digit Pattern Code for QTP, ROM (blank otherwise)	

Examples:

a) PIC16C54A -04/P 301 = Commercial temp., PDIP package, 4MHz, normal VDD limitis, QTP pattern #301.

b) PIC16LC58A - 04I/SO = Industrial temp., SOIC package, 4MHz, Extended VDD limits.

c) PIC16CR54A - 10I/P355 = ROM program memory, Industrial temp., PDIP package, 10MHz, normal VDD limits.

Note 1: b = blank

2: C = Standard VDD range
LC = Extended VDD range
CR = ROM Version, Standard VDD range
LCR = ROM Version, Extended VDD range
LV = Low Voltage VDD range

3: T = in tape and reel - SOIC, SSOP packages only.

4: UV erasable devices are tested to all available voltage/frequency options. Erased devices are oscillator type 04. The user can select 04, 10 or 20 oscillators by programmng the appropriate configuration bits.

PIC16C54/55/56/57 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information (e.g., on pricing or delivery) refer to the factory or the listed sales office.

PART NO.	-XX	X	/XX	XXX
Device	Oscillator Type	Temperature Range	Package	Pattern

Device	PIC16C54, PIC16C54T(2) PIC16C55, PIC16C55T(2) PIC16C56, PIC16C56T(2) PIC16C57, PIC16C57T(2)	
Oscillator Type	RC	= Resistor Capacitor
	LP	= Low Power Crystal
	XT	= Standard Crystal/Resonator
	HS	= High Speed Crystal
	10	= 10 MHz Crystal
	b(1)	= No type for JW(3) devices
Temperature Range	b(1)	= 0°C to +70°C (Commercial)
	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Automotive)
Package	JW	= Windowed CERDIP
	P	= PDIP
	S	= Die in Waffle Pack
	SO	= SOIC (Gull Wing, 300 mil body)
	SP	= Skinny PDIP (28 pin, 300 mil body)
	SS	= SSOP (209 mil body)
Pattern	3-digit Pattern Code for QTP (blank otherwise)	

Examples:

a) PIC16C54 - XT/PXXX = "XT" oscillator, commercial temp., PDIP, QTP pattern.

b) PIC16C55 - XTI/SO = "XT" oscillator, industrial temp., SOIC (OTP device)

c) PIC16C55 /JW = Commercial temp. CERDIP with window.

d) PIC16C57 - RC/S = "RC" oscillator, commercial temp., dice in waffle pack.

Note 1: b = blank

2: T = in tape and reel - SOIC, SSOP packages only.

3: UV erasable devices are tested to all available voltage/frequency options. Erased devices are oscillator type RC. The user can select RC, LP, XT or HS oscillators by programming the appropriate configuration bits.

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see below)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.
For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

NOTES:

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 602-786-7200 Fax: 602-786-7277
Technical Support: 602 786-7627
Web: http://www.microchip.com

Atlanta
Microchip Technology Inc.
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston
Microchip Technology Inc.
5 Mount Royal Avenue
Marlborough, MA 01752
Tel: 508-480-9990 Fax: 508-480-8575

Chicago
Microchip Technology Inc.
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
Microchip Technology Inc.
14651 Dallas Parkway, Suite 816
Dallas, TX 75240-8809
Tel: 972-991-7177 Fax: 972-991-8588

Dayton
Microchip Technology Inc.
Two Prestige Place, Suite 150
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit
Microchip Technology Inc.
42705 Grand River, Suite 201
Novi, MI 48375-1727
Tel: 248-374-1888 Fax: 248-374-2874

Los Angeles
Microchip Technology Inc.
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 714-263-1888 Fax: 714-263-1338

New York
Microchip Technology Inc.
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 516-273-5305 Fax: 516-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

AMERICAS (continued)

Toronto
Microchip Technology Inc.
5925 Airport Road, Suite 200
Mississauga, Ontario L4V 1W1, Canada
Tel: 905-405-6279 Fax: 905-405-6253

ASIA/PACIFIC

Hong Kong
Microchip Asia Pacific
RM 3801B, Tower Two
Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2-401-1200 Fax: 852-2-401-3431

India
Microchip Technology Inc.
India Liaison Office
No. 6, Legacy, Convent Road
Bangalore 560 025, India
Tel: 91-80-229-0061 Fax: 91-80-229-0062

Japan
Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa 222-0033 Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Shanghai
Microchip Technology
RM 406 Shanghai Golden Bridge Bldg.
2077 Yan'an Road West, Hong Qiao District
Shanghai, PRC 200335
Tel: 86-21-6275-5700 Fax: 86 21-6275-5060

ASIA/PACIFIC (continued)

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan, R.O.C
Microchip Technology Taiwan
10F-1C 207
Tung Hua North Road
Taipei, Taiwan, ROC
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

United Kingdom
Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44-1189-21-5858 Fax: 44-1189-21-5835

France
Arizona Microchip Technology SARL
Zone Industrielle de la Bonde
2 Rue du Buisson aux Fraises
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Arizona Microchip Technology GmbH
Gustav-Heinemann-Ring 125
D-81739 Müchen, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy
Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-39-6899939 Fax: 39-39-6899883

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